P.E.S. COLLEGE OF ENGINEERING, MANDYA

(AN AUTONOMOUS INSTITUTION AFFILIATED TO VTU, BELAGAVI)

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEM

SCHEME AND SYLLABUS

2024– 25

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

P.E.S COLLEGE OF ENGINEERING, MANDYA-571401

KARNATAKA

Vision

PESCE shall be a leading institution imparting quality engineering and management education developing creative and socially responsible professionals.

Mission

- Provide state of the art infrastructure, motivate the faculty to be proficient in their field of Specialization and adopt best teaching-learning practices.
- Impart engineering and managerial skills through competent and committed faculty using Outcome based educational curriculum.
- Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the societal needs.
- Promote research, product development and industry-institution interaction.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

About the Department:

The department of Electronics and Communication Engineering was incepted in the year 1967 with an undergraduate program in Electronics and Communication Engineering. Initially program had an intake of 60 students and presently 150 students graduate every year. The long journey of 50 years has seen satisfactory contributions to the society, nation and world. The alumni of this department have strong global presence making their alma mater proud in every sector they represent.

Department has started its PG program in the year 2012 in the specialization of VLSI design and Embedded systems. Equipped with qualified and dedicated faculty department has focus on VLSI design, Embedded systems and Image processing. The quality of teaching and training has yielded high growth rate of placement at various organizations. Large number of candidates pursuing research programs (M.Sc/Ph D) is a true testimonial to the research potential of the department.

Vision

The department of E & C would endeavour to create a pool of engineers who would be **extremely competent technically, ethically strong** also fulfil their obligation in terms of **social responsibility**.

Mission

- **M1:** Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience conducive to imbibe technical knowledge and practicing ethics.
- **M2**:Group and individual exercises to inculcate habit of analytical and strategic thinking to help the students to develop creative thinking and in still team skills
- **M3**:MoUs and Sponsored projects with industry and R & D organizations for Collaborative learning.
- **M4**: Enabling and encouraging students for continuing education and moulding them for life-long learning process.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(A) Programme Learning Objectives (PLOs)

M.Tech in VLSI Design and Embedded system during two years term, aims to

1. Provide the students with strong fundamental and advanced knowledge in VLSI design and Embedded system with an emphasis to solve engineering problems.
2. Train the students in VLSI and Embedded system design tools and make them fit for the industries.
3. Inculcate in students the professional and ethical attitude, effective Communication skills, team spirit and nurture them as leaders.
4. Provide teaching skills and inculcate spirit of research.
5. Motivate to continue education leading to doctoral degree and choose research as Career option.

(B) Programme educational outcomes

The objectives aim to produce qualified Electronic Engineering Post-graduates who will:

PEO 1: Identify and apply appropriate Electronic Design Automation (EDA) to solve real world problems in VLSI and Embedded Systems domain to create innovative products and systems.

PEO 2: Develop managerial skill and apply appropriate approaches in the domains of VLSI design and Embedded Systems incorporating safety, sustainability and become a successful professional or an Entrepreneur in the domain.

PEO 3: To exhibit professional competence and leadership qualities with harmonious blend of ethics leading to an integrated personality development.

(C)Program Specific Outcomes:

PSO-1: An ability to understand the basic concepts in VLSI DESIGN AND EMBEDDED SYSTEMS and to apply them in the design and implementation of VLSI AND EMBEDDED CIRCUITS

PSO-2: An ability to solve complex problems in VLSI DESIGN AND EMBEDDED SYSTEMS, using latest hardware and software tools, along with analytical skills to arrive at appropriate solutions.

(D) Programme Outcomes (POs):

The Master of Technology Programme in Electronics and Communication Engineering [M.Tech in VLSI Design and Embedded systems] must demonstrate that its Post graduates have

PO1: Ability to solve multidisciplinary problems using VLSI circuits in multiple ways and provide optimized solutions.

PO2: Demonstrate a degree of mastery over the area of VLSI Design and Embedded Systems. The mastery should be a level higher than the requirements of the bachelor's in electronics &communication engineering program.

PO3: Ability to use techniques and modern CAD tools so as to implement them in engineering practice to develop professional skills that will prepare the students for immediate employment in the relevant branch of engineering in industry.

PO4: Acquire professional and intellectual integrity, research ethics and execute socio-concern projects related to modern VLSI and embedded systems

PO5: Write and present a substantial technical report/document in the field of VLSI design and embedded systems

I – Semester										
Sl. No.	Course Type	Course Code	Course Title	Teaching Hours/Week			Examination Marks			Credits
				Theory	Practical/ Seminar	Tutorial/ SDA	CIE	SEE	Total	
				L	P	T/SDA				
1.	IPCC	P24MECE11	System Verilog	3	2	0	50	50	100	4
2.	PCC	P24MECE12	Advanced Machine Learning and Deep Learning	3	0	0	50	50	100	3
3.	PCC	P24MECE13	Digital Circuits and Logic Design	3	0	0	50	50	100	3
4.	PEC	P24MECE14X	Professional Elective I	3	0	0	50	50	100	3
5.	PEC	P24MECE15X	Professional Elective II	3	0	0	50	50	100	3
6.	PCL	P24MECL16	VLSI Design Lab	0	1	1	50	50	100	2
7.	NCMC	P24MRMI17	Research Methodology and IPR(**Online**)		Online courses(online.vtu.ac.in)					PP
Total							**300**	**300**	**600**	**18**

Note: PCC: Professional Core Course | IPCC-Integrated Professional Core Courses |PEC- Professional Elective Course| NCMC-Non Credit Mandatory Course | PECL - Professional Elective Lab

Professional Elective - I			Professional Elective - II		
Sl. No	**Course Code**	**Course Title**	**Sl. No**	**Course Code**	**Course Title**
1.	P24MECE141	ASIC Design	1.	P24MECE151	Advance Embedded Systems
2.	P24MECE142	Advanced Computer Networking	2.	P24MECE152	Advanced Wireless Communication
3.	P24MECE143	Advanced Signal Processing	3.	P24MECE153	Multimedia and Applications
4.	P24MECE144	Power Converters	4.	P24MECE154	Process Control

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **SYSTEM VERILOG**		
Course Code: **P24MECE11**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:2	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3	
Credits:**04**		
Prerequisite:		
Digital Logic Design, Verilog, VLSI Testing and Verification		
Course learning Objectives:		
CLO1:Understand Digital System Verification Using Object Oriented Methods CLO2: Learn the System Verilog Language for Digital System Verification. CLO3: Create/Build Test Benches for the Design/Methodology. CLO4: Use Constrained Random Tests for Verification CLO5: Understand Concepts of Functional Coverage		
UNIT -1		8 Hours
Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench. **Data Types**: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With type def, Creating User Defined Structures, Type Conversion, Enumerated Types, Constants and Strings, Expression Width.		
Self-Study Content: Analyse the Difference between Verilog and System Verilog Data types		
Textbook Map: Chapter-1 : 1.1,1.3-1.10 Chapter-2 : 2.1-2.9, 2.11,2.13-2.16		
Teaching Learning Process: PPT,		
UNIT 2:		8 Hours
Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. **Connecting the Test Bench and Design**: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.		
Self-Study Content: Develop a System Verilog Code for Conditional Circuits using Procedural Statements		
Textbook Map: Chapter-3 :3.1-3.7 Chapter 4: 4.1-4.4, 4.9		
Teaching Learning Process: PPT		
UNIT 3:		8 Hours
Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, In Line Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.		
Self-Study Content: Understand the basic OOPs Concepts		
Textbook Map: Chapter-6.1,6.3-6.8,6.10,6.12,6.15,6.16		
Teaching Learning Process: PPT		
UNIT 4:		8 Hours
Threads and Inter process Communication: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, Building A Test Bench with Threads and Inter Process Communication.		

Self-Study Content: Analyse the usage of Inheritance in System Verilog				
Textbook Map: Chapter-7				
Teaching Learning Process: PPT				
UNIT 5:				8 Hours
Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggering a Cover Group, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, Measuring Coverage Statistics During Simulation.				
Self-Study Content: Case study of ALU for Functional Coverage				
Teaching Learning Process: PPT				
Textbook Map: Chapter-9				
Course Outcomes: At the end of the course students should be able to :				
CO1: Apply the System Verilog concepts to verify the design. CO2: Apply constrained random tests benches using System Verilog. CO3: Appreciate Functional Coverage				
Suggested Learning Resources:				
Textbooks:				
1.	Title	Author	Year & Edition	Publisher
1	System Verilog for Verification–A guide to learning the Testbench language features	ChrisSpear	Second Edition, 2010	Springer Publications
2	System Verilog for Design-A guide to using system Verilog for Hardware design and modelling	Stuart Sutherland, Simon Davidmann, Peter Flake	Second Edition, 2006	Springer Publications
Reference Books:				
1.	System Verilog for Design	Stuart Sutherland	2nd edition, 2006	Springer Publications
2.	System Verilog Assertions	Vijaya Raghavan	2014	Springer Publications
Web links and Video Lectures (e-resources)				
1.https://www.youtube.com/watch?v=N9cdUhdNrgg&list=PLqPfWwayuBvOL920Q8ljlVmUMHshb5lJE				
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)				
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing				

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **SYSTEM VERILOG**		
Course Code: **P24MECE11**	CIE Marks: 50	CIE Weightage: 50
Teaching hours/week (L:T:P)3:0:2	SEE Marks:100	SEE Weightage:50
Teaching hours of Pedagogy:40	Exam Hours: 3	
Credits: 04		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes:	**Expected Bloom's Level**	**Program Outcomes**
CO1: Apply the System Verilog concepts to verify the design.	L2, L3	PO1, PO3, PO4, PO5
CO2: Apply constrained random tests benches using System Verilog.	L3,L4	PO1, PO4, PO5
CO3: Appreciate Functional Coverage.	L2,L3	PO1,PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3		1	1	2		
CO2	2			1	2		
CO3	2			1			

PRACTICAL COMPONENT OF IPCC Using simulation software Vivado	
1.	Develop a System Verilog code to simulate and verify the operation of a tri state buffer.
2.	Using function facilities of SystemVerilog develop a code forgiven arithmetic/logical operation and verify its operation through its test bench simulation.
3.	Using task facility of System Verilog develop a code to synthesize given logical functionality, verify its operation through test bench and also comment on synthesizability with respect to return type.
4.	Using class data types in System Verilog develop a code for control register with given specifications and simulate its operation.
5.	Develop a System Verilog code to illustrate the concept of threads and fork.
6.	Develop a System Verilog code to create semaphores for controlling the register access.
7.	Using randomization facility in System Verilog develop a test bench to verify the operation of a given logic design.
8.	Using Enumerated type facility in System Verilog develop a code to simulate the operation of a traffic control state machine.

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED MACHINE LEARNING AND DEEP LEARNING**		
Course Code**: P24MECE12**	CIE Marks:50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40 hrs	Exam Hours: 03(Theory)	
Credits: **03**		
Prerequisite:		
Basic operating understanding of calculus, matrices and Python programming. And provide extensive mathematical background, in linear algebra may also be helpful in navigating certain sections of mathematical exposition. Knowledge of neural network architecture and design.		
Course Learning Objectives: CLO1: To understand the fundamental concepts of machine learning and its applications. CLO2: To master the concepts of classification and clustering techniques. CLO3: To develop a deep understanding of convolutional neural networks (CNNs) and their architecture. CLO4: To apply deep learning techniques to large-scaled at a sets and real-world problems.		
UNIT -1		8 Hours
The Neural Network: Building Intelligent Machines, Limits of Traditional Computer Programs, Mechanics of Machine Learning, Neuron, Expressing Linear Perceptron's as Neurons, Feed-Forward Neural Networks, Linear Neurons and Their Limitations, Sigmoid, Tanh, and ReLU Neurons, Soft max Output Layers. **Training Feed-Forward Neural Networks**: Fast-Food Problem, Gradient Descent, Delta Rule and Learning Rates, Gradient Descent with Sigmoidal Neurons, Back propagation Algorithm, Stochastic and Mini batch Gradient Descent, Test Sets, Validation Sets, and Over fitting, Preventing Over fitting in Deep Neural Networks. **RBT Levels:** L2, L3		
Self-Study Content:1. Study the basic intuition for machine learning. 2. Discuss the basic structure of a neuron, how feed-forward neural networks works.		
Textbook 1 Map: 1.1 to 1.10 and 2.1 to 2.8		
Teaching Learning Process: Power point presentation with demonstration (MAT LAB or Python) or any violable tool.		
UNIT 2:		8 Hours
Beyond Gradient Descent: Challenges with Gradient Descent, Local Minima in the Error Surfaces of Deep Networks, Model Identifiability, Flat Regions in the Error Surface, When the Gradient Points in the Wrong Direction, Momentum-Based Optimization, Brief View of Second-Order Methods, Learning Rate Adaptation, AdaGrad—Accumulating Historical Gradients, RMSProp—Exponentially Weighted Moving Average of Gradients, Adam—Combining Momentum and RMSProp, Philosophy Behind Optimizer Selection. **RBT Levels:** L3		
Self-Study Content: 1. Identify the challenges that arise when trying to train deep networks with complex error surfaces. 2.Understand how momentum can be used to overcome ill-conditioning.		
Textbook 1 Map: 4.1 to 1.10		
Teaching Learning Process: Power point presentation with demonstration (MAT LAB or Python) or any violable tool.		

UNIT 3:	8 Hours
Convolutional Neural Networks: The operation, Pooling, Convolution and Pooling as an infinitely strong prior, Variants of the basic functions, efficient algorithms, Random or Unsupervised Features, Neuro scientific Basis for Convolutional Networks. **RBT Levels:** L3	
Self-Study Content: 1. Identify the applications of convolution neural networks. 2. Develop a python code for Efficient Convolution Algorithms.	
Textbook 2 Map:9.1 to 9.5, 9.8 to 9.10	
Teaching Learning Process: Power point presentation with case studies and/or demonstration (MAT LAB or Python) or any violable tool.	
UNIT 4:	8 Hours
Neural Networks: RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated Optimization for Long Term Dependencies. **RBT Levels:** L3	
Self-Study Content: 1.Understand the concept of multi-layer networks of Recurrent Neural Networks. 2. Identify the different Long Short Term Memory and other Gated RNNs.	
Textbook 2 Map: 10.2 to 10.6, 10.10 to 10.11	
Teaching Learning Process: Power point presentation and guest lecture.	
UNIT 5:	8 Hours
Applications: Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications. **RBT Levels:** L3,L4	
Self-Study Content: 1. Discuss how to use deep learning to solve applications in computer vision, speech recognition, natural language processing, and other application areas of commercial interest	
Textbook 2 Map: 12.1 to 12.5	
Teaching Learning Process: Power point presentation and seminar.	
Course Outcomes: At the end of the course students should be able to :	
CO1: **Illustrate** the principles and mechanism of working of neural networks. CO2: **Analyze** the effectiveness of neural networks and their architectures in solving a problems. CO3: **Develop** a neural network/machine learning model to solve given problem.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Fundamentals of Deep Learning	Nikhil Budama	2017, 1st Edition	O'Reilly Media, Inc, USA ISBN-10 9781491925614 ISBN-13978-1491925614
2	Deep Learning	Goodfellow, Bengio and Courville	2018	The MIT Press,2016,800 pp,ISBN:0262035618
Reference Books:				
1.	Neural Networks and Deep Learning	CharuAggarwal	2018	

2.	Hands-on Deep Learning Algorithms with Python	Sudharsan, Ravichandran	2019	

Web links and Video Lectures (e-resources)
1. https://nptel.ac.in/
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title:**ADVANCED MACHINE LEARNING AND DEEP LEARNING**		
Course Code: **P24MECE12**	CIE Marks:50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40 hrs	Exam Hours: 03(Theory)	
Credits: 03		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Illustrate the principles and mechanism of working of neural networks.	L2	PO1
CO2: Analyze the effectiveness of neural networks and their architectures in solving problems.	L3	PO2
CO3: Develop a neural network/machine learning model to solve given problem**.**	L5	PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3			2				2

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **DIGITAL CIRCUITS AND LOGIC DESIGN**		
Course Code: **P24MECE13**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P:): 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	
Credits**:03**		
Prerequisite:		
Electric Circuits, Microelectronics, Digital Systems.		
Course learning Objectives:		
CLO1: Understand the concepts of sequential machines. CLO2: Apply fault detection experiments to sequential circuits. CLO3: Analyze the faults in the design of circuits. CLO4: Design Sequential Machines/Circuits		
UNIT -1		8 Hours
Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks **Capabilities, Minimization, and Transformation of Sequential Machines:** The Finite-State Model, Further Definitions, Capabilities		
Self-Study Content: State equivalence and machine minimization		
Textbook Map 1: 7.1,7.2 10.1,10.2		
Teaching Learning Process: Poster presentation/Quiz/Seminar/Team demonstration		
UNIT 2:		8 Hours
Testing of Combinational Circuits: Fault models, Structural testing, I_{DDQ} testing, Delay fault testing, Synthesis for testing, Testing for nanotechnologies.		
Self-Study Content: Fault Diagnosis of Digital Circuits		
Textbook Map 1: 8.1, 8.2, 8.3, 8.4, 8.5,8.6		
Teaching Learning Process: Flip class/Quiz/Seminar/Team demonstration		
UNIT 3:		8 Hours
Introduction to Synchronous Sequential circuits and iterative networks: Sequential circuits-introductory example, The finite- state model-basic definitions, Memory elements and their excitation functions, Synthesis of synchronous sequential circuits, An example of a computing machine		
Self-Study Content: Iterative Networks		
Textbook Map 1: 9.1, 9.2, 9.3, 9.4, 9.5		
Teaching Learning Process: Quiz/Seminar/Team demonstration/One minute paper writing		
UNIT 4:		8 Hours
Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.		
Self-Study Content: Built-in self-test (BIST)		
Textbook Map 1: 12.1,12.2,12.3,12.4,12.5,12.6,12.7,12.8,12.9		
Teaching Learning Process: One minute paper writing/ Quiz/Seminar/Team demonstration		
UNIT 5:		8 Hours
Faults in Digital Circuits: Failures and faults, Modelling of faults, Stuck-At-Faults,		

Bridging faults, Breaks and Transistor Stuck-On/-Open faults in CMOS, Delay faults.
Test Generation for Sequential Circuits: Testing of Sequential Circuits as Iterative Combinational Circuits, State Table Verification, Test Generation Based on Circuit Structure, Functional Fault Models

Self-Study Content: Test Generation Based on Functional Fault Models

Teaching Learning Process: Think pair share/One minute paper writing/ Quiz/Seminar

Textbook Map 2: 1.1, 1.2, 1.2.1, 1.2.2, 1.2.3,1.2.4, 1.3, 4.1,4.2,4.3,4.4.

Course Outcomes: At the end of the course students should be able to :

CO1:Apply electronics circuit knowledge to understand digital circuits.
CO2:Analyze digital circuits for faults using various methods.
CO3: Design the fault detection circuit for synchronous sequential circuits.
CO4:Simulate fault models with available tools.

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1	'Switching and Finite Automata Theory'	ZviKohavi		ISBN:978_0_07_099387_7 2ndEdition ,2008.
2	'Digital Circuit Testing and Testability'	Parag K Lala		Academic Press

Reference Books:

1.	Digital Circuits and logic Design', Charles RothJr	Parag K Lala	PrenticeHallInc.1 985.	
2.	'Introductory Theory of Computer'	E.V.Krishnamu rthy	1983	Macmillan PressLtd
3	Fault Tolerant and Fault Testable Hardware Design'	Parag K Lala	1985.	Prentice HallInc.
4	Theory of computer science–Automata, Languages and Computation	Mishra & Chandrasekara n,	2ndEdition, PHI, 2004.	

Web links and Video Lectures (e-resources)

1. https://nptel.ac.in/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **DIGITAL CIRCUITS AND LOGIC DESIGN**		
Course Code: **P24MECE13**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P:): 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03(Theory)	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Apply knowledge of electronics circuit to understand the concepts of digital circuits.	L1	PO1
CO2: Analyse the faults in the digital circuits using various methods.	L2	PO2
CO3: Design the fault detection circuit for synchronous sequential circuits.	L5	PO2
C04: Simulate fault models with available tools.	L5	PO3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3						3
CO2		3					3
CO3		2				2	
CO4			2				

PROFESSIONAL ELECTIVE I		
PART A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ASIC DESIGN**		
Course Code: **P24MECE141**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3Hrs	
Credits: 03		
Prerequisite: • Basic Semiconductor Concepts. • Digital Logic Design. • HDL (Hardware Description Language). • EDA Tools (Electronic Design Automation). • Simulation and Verification.		
Course learning Objectives:		
CLO1: To learn ASIC methodologies and programmable logic cells to implement a function on IC. CLO2: To analyze back-end physical design flow, including partitioning, floor-planning, placement, and routing. CLO3: To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs		
UNIT -1		8 Hours
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic**: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.		
Self-Study Content: Case Study, Carry out the survey on ASIC ICs which are used in industries.		
Textbook Map: Text 1: 1.1.1,1.1.2,1.1.7, 1.2,1.5,2.6(2.6.1,2.6.2,6.2.3,2.6.4,2.6.6),2.8.		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, ActedACT:ACT1, ACT2andACT3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/OBlock.		
Self-Study Content: Other Data path Operators, Library Architecture, Gate array Design.		
Textbook Map:3.3,3.4,5.1(5.1.3,5.1.4),5.2.1,5.3,5.4,6.7		
Teaching Learning Process: Seminar		
UNIT 3:		8 Hours
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction**: Physical Design, CAD Tools, System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.		
Self-Study Content: Schematic –Entry tools and Back annotation.		
Textbook Map: Text 1: 9.1(9.1.1 to 9.1.11), 15.1,15.2,15.3,15.4,15.7 (15.7.1,15.7.3,15.7.4, 15.7.5,15.7.7)		

Teaching Learning Process: Seminar	
UNIT 4:	8 Hours
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	
Self-Study Content: Introduction to Synthesis and Simulation.	
Textbook Map: Text 1: 16.1,16.2.2,16.2.16.2.4,16.2.6,16.2.8,16.3	
Teaching Learning Process: Paper Presentation	
UNIT 5:	8 Hours
Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	
Self-Study Content: Partitioning methods, Global Routing, Detail Routing, Special Routing.	
Textbook Map: Text1: 17.1(17.1.1,17.1.3,17.1.4,17.1.7), 17.2(17.2.1,17.2.2,17.2.4, 17.2.6, 17.2.7, 17.2.8,17.2.9)17.3,17.4	
Teaching Learning Process: Paper Presentation	
Course Outcomes: At the end of the course students should be able to :	
CO1: Describe the concepts of ASIC design methodology, data path elements, logical effort. CO2: Analyze the design of ASICs suitable for specific tasks, perform design entry and Explain the physical design flow. CO3: Design data path elements for ASIC cell libraries and compute optimum path delay. CO4:Create floor plan including partition and routing with the use of CAD algorithms	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	"**Application - Specific Integrated Circuits**"	M.J.S .Smith	1st Edition, 2003.ISBN-13: 978-8177584080.	Pearson Education
Reference Books:				
1.	**"CMOS VLSI Design: A Circuits and Systems Perspective"**	Neil H.E. Weste, David Harris, and Ayan Banerjee	3rdedition, 2011	Addison Wesley/ Pearson education
2.	**"VLSI Design: A Practical Guide for FPGA and ASIC Implementations"**	Vikram Arkalgud Chandrasetty	ISBN: 978-1-4614-1119-2.2011	Springer
3.	**"An ASIC Low Power Primer"**	RakeshChadha,BhaskerJ,	ISBN:978-14614-4270-7.	Springer
4.	**"Digital Design (Verilog):An Embedded Systems Approach Using Verilog"**	PeterJ.Ashenden	1stEdition	Kindle Edition

Web links and Video Lectures (e-resources)
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **ASIC DESIGN**		
Course Code: **P24MECE141**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3Hrs	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Describe the concepts of ASIC design methodology, data path elements, logical effort.	L1	PO1
CO2: Analyze the design of ASICs suitable for specific tasks, perform design entry and Explain the physical design flow.	L2	PO2,3
CO3: Design data path elements for ASIC cell libraries and compute optimum path delay.	L5	PO3
CO4: Create floor plan including partition and routing with the use of CAD algorithms.	L5	PO4
CO5: Design CAD algorithms and explain how these algorithms interact in ASIC design.	L5	PO3,4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	**2**					**2**	
CO2		**2**	**2**				
CO3			**3**				
CO4			**3**				**1**
CO5			**2**	**2**			

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED COMPUTER NETWORKING**		
Course Code: **P24MECE142**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy: 40	Exam Hours: 3	
Credits: **03**		
Prerequisite:		
A secure Internet connection from the Internet Service Provider (ISP), A router with a high-speed Internet connection, A modem, Firewall capabilities, One or more switches (allows computers to link to one another over an internal network), Phone line/cable/fiber optic linking (wired or wireless)		
Course learning Objectives:		
CLO1:This course focuses on advanced networking concepts for next generation network architecture and design CLO2:It covers SDN and virtualization for designing next generation networks		
UNIT -1		8 Hours
MEDIUM ACCESS CONTROL SUB LAYER: Wireless LANs, Broadband Wireless, Bluetooth, RFID. THE NETWORK LAYER: Network Layer Design Issues, Congestion Control Algorithms, Quality of Service, The Network Layer in the Internet.		
Self-Study Content: Technical terminology used in Computer Networking and Internet working.		
Textbook Map:(Text Book 1: 4.4, 4.5, 4.6, 4.7,5.1, 5.3, 5.4, 5.6.3 to 5.6.9) (RBT Levels: L1 & L2)		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
THE APPLICATION LAYER: The Domain Name System, Electronic Mail, The World Wide Web.		
Self-Study Content: Recent concepts of Application Layer		
Textbook Map:(Text Book 1: 7.1, 7.2, 7.3) (RBT Levels: L1 & L2)		
Teaching Learning Process: Seminar/ poster Presentation		
UNIT 3:		8 Hours
SOFTWARE DEFINED NETWORK (SDN): Evolution of Switches and Control Planes, Cost, SDN Implications for Research and Innovation GENESIS OF SDN: The Evolution of Networking Technology, Forerunners of SDN, Software Defined Networking is Born, Sustaining SDN Interoperability, Open Source Contributions, Network Virtualization HOW SDN WORKS: Fundamental Characteristics of SDN, SDN Operation, SDN Devices, SDN Controller, SDN Applications, Alternate SDN Methods		
Self-Study Content: Important components of SDN controllers		
Textbook Map: (Text Book 2: 2.1, 2.2, 2.3, 3.1, 3.2, 3.4, 3.5, 3.6, 3.7, 4.1 to 4.6) (RBT Levels: L1 & L2)		

Teaching Learning Process: Individual Role play/Team Demonstration/ Collaborative Activity	
UNIT 4:	8 Hours
THE OPENFLOW SPECIFICATION: Open Flow Overview, Open Flow 1.0 and Open Flow Basics, Open Flow Additions - 1.1, 1.2, 1.3, 1.4, 1.5, Improving Open Flow Interoperability, Optical Transport Protocol Extensions, Open Flow Limitations	
Self-Study Content: Differentiate between SDN and open flow	
Textbook Map:(Text Book: 2 Chapter 5) (RBT Levels: L1& L2)	
Teaching Learning Process: Case study	
UNIT 5:	8 Hours
NETWORK FUNCTIONS VIRTUALIZATION: Definition of NFV, Virtualize, Standards, OPNFV, Leading NFV Vendors, SDN Vs NFV, In-Line Network Functions. SDN OPEN SOURCE: SDN Open Source Landscape, The OpenFlow Open Source Environment, Profiles of SDN Open Source Users, OpenFlow Source Code, Switch Implementations, Controller Implementations, SDN Applications, Orchestration and Network Virtualization, Simulation, Testing and Tools, Open Source Cloud Software, Example: Applying SDN Open Source.	
Self-Study Content: Recent updates & study on physical components of Computer network	
Teaching Learning Process: Learn by Doing	
Textbook Map:(Text Book 2: 10.1-10.7 & 13.1, 13.2, 13.5 - 13.13) (RBT Levels: L1 & L2)	
Course Outcomes: At the end of the course students should be able to :	
CO1: Understand advanced concepts and next generation networks. CO2: Analyze network Algorithm's, Protocols and their functionalities. CO3: Comprehend features of SDN and its application to next generation Systems	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Computer Network	Andrew S. Tanenbaum, David J. Wetherall	5th Edition	Pearson Education
2	Software Defined Networks – A Comprehensive Approach	Paul Goransson, Chuck Black and Timothy Culver	2nd Edition, 2017	Morgan Kaufmann
Reference Books:				
1.	Data Communications and Networking	Behrouz A. Forouzan	Fourth Edition,2007	Tata McGraw Hill
2.	Computer Networking- A Top down Approach Featuring the Internet	James F Kurose, Keith W Ross	7th Edition, 2017	Pearson Education

Web links and Video Lectures (e-resources)
https://onlinecourses.nptel.ac.in>noc23_cs35
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class

2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED COMPUTER NETWORKING**		
Course Code: **P24MECE142**	CIE marks: 50	CIE Weightage:50%
Teaching hours/weeks (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy 40 hrs	Exam hours: 3	
Credits**: 03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Understand advanced concepts and next generation networks.	L1	PO1,PO2,PO4
CO2: Analyze network Algorithm's, Protocols and their functionalities.	L2	PO1,PO2,PO3,PO4,PO5
CO3: Comprehend features of SDN and its application to next generation systems	L3	PO1,PO2,PO3,PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3	2		2			
CO2	3	3	2	3	2		
CO3	2	2	2		2		

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title:**ADVANCED SIGNAL PROCESSING**		
Course Code**: P24MECE143**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hrs	
Credits:**03**		
Prerequisite:		
Signals & Systems, Digital Signal Processing.		
Course learning Objectives:		
CLO1: Explore & understand algorithms & techniques of Signal processing in context real time applications. CLO2: Learn analysing discrete time signals &systems. CLO3: Design Sub-blocks of signal processing systems. CLO4: Apply the knowledge of signals & algorithms in developing signal processing blocks.		
UNIT -1		8 Hours
Analysis of Discrete Time Signals: Basic elements of a DSP System –Review of Sampling and Quantisation – Sampling theorem for low pass and band pass signals, uniform and non-uniform quantization, Application of quantisation in lossy compression of signals – Lloyd Max quantizer; Fourier analysis of Continuous and Discrete time signals – Review of Fourier series and Fourier transform, Discrete Time Fourier Transform(DTFT),Discrete Fourier Transform (DFT), Interpretation of DFT Spectrum, Review of DFT properties –Convolution and correlation, Convolution of long sequences, Leakage effect, Windowing – Introduction to other transforms : Discrete Cosine Transform (DCT), Walsh Hadamard Transform (WHT), Karhunen Loeve Transform (KLT) – Applications. **RBTLevels:**L2,L3		
Self-Study Content: Walsh Hadamard Transform (WHT)– Applications		
Textbook Map: Text 1-2.1-2.13,3.1-3.7		
Teaching Learning Process: power point presentation with demonstration(MATLAB Simulation)		
UNIT 2:		8 Hours
Digital Filters and Implementation: Review of FIR and IIR filter design – Notch filter– Comb filter– All pass filters – Applications – Structures for digital filter realization: Signal flow graph and block diagram representations, FIR and IIR Filter structures, Lattice structures – Finite word length effects – Fixed-point and floating-point DSP arithmetic, Effects of quantization, Scaling, Limit cycles in fixed point realizations of IIR digital filters, Limit cycles due to overflow. Quantization effect in DFT and FFT computation. **RBTLevels:**L3,L4		
Self-Study Content: Quantization effect in DFT and FFT – Applications		
Textbook Map: Text 1-4.1-4.11.		
Teaching Learning Process: power point presentation with Case Studies.		
UNIT 3:		8 Hours
Multirate Signals and Systems: Introduction to multirate signal processing with applications, Multirate System Fundamentals – Decimation and Interpolation, Transform domain analysis of Decimators and Interpolators, Decimation and Interpolation filters, Fractional sampling rate alteration, Practical sampling rate converter design.		

RBTLevels:L3,L4	
Self-Study Content: Decimation and Interpolation – Applications	
Textbook Map: Text 2-2.1-2.8,3.1-3.7	
Teaching Learning Process: power point presentation with guest lecturer.	
UNIT 4:	8 Hours
Introductionto2-DSignalsandSystems: Polyphase decomposition and efficient structures – Introduction to digital filter banks – The DFT filter bank, Two Channel Quadrature Mirror Filter bank (QMF), Perfect Reconstruction.	
Self-Study Content: DFT filter bank – Applications	
Textbook Map: Text 3-1.1-1.8.	
Teaching Learning Process: power point presentation with examples.	
UNIT 5:	8 Hours
Introduction to2-D Signals and Systems: Elementary 2D signals–Linear shift Invariant systems–Separability – 2Dconvolution–Introductionto2Dtransforms:2DDFT,2DDCT, Applications. **RBTLevels:**L3,L4	
Self-Study Content: 2Dconvolution– Applications	
Teaching Learning Process: power point presentation with examples.	
Textbook Map: Text 3-2.1-2.8,3.1-3.3	
Course Outcomes: At the end of the course students should be able to :	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Digital Signal Processing: Principles, Algorithms and Applications,	John G. Proakis, Dimitris G. Manolakis	2007, 4thEdition	Pearson India
2	Multirate systems and filter banks	P.P.Vaidyanathan	1992, 2ndEdition	Pearson Education India
	Two dimensional signal and image processing	LimJ.S	1990.	Prentice Hall
Reference Books:				
1.	Digital Signal Processing: Theory and Practice	K Deergha Rao,MNS Swamy	2018.	Springer
2.	The Scientist and Engineer's Guide to Digital Signal Processing	StevenW.Smith	1999	California
3.	Digital Signal Processing: A Computer Based Approach	MitraS.K	2013	McGraw-Hill Publishing Company

Web links and Video Lectures (e-resources)
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)
1. Flip Class 2. Seminar/ poster Presentation

3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing

PART-B		
Academic year:2024-25	**Semester:**I	**Scheme:**P24
Course Title: : **ADVANCED SIGNAL PROCESSING**		
Course Code: P24MECE143	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hrs	
Credits:03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Analyze the effect of sampling and quantisation of signals and appraise its relevance with reference to applications.	L2	PO1
CO2: Formulate various transform domain representationsof1Dand2Dsignalsand demonstrate their applications with reference to practical signals.	L4	PO1
CO3: Examine finite word length effects in real time signal processing.	L2	PO3
CO4: Illustrate the effect of sampling rate converters and design distortion free digital filter banks illustrating their applications to process real life signals.	L2	PO3
CO5: Identification & design of DSP architectures for given requirements.	L5	PO2

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2					2	
CO2	2					2	
CO3			1				
CO4			1				
CO5		2					2

PROFESSIONAL ELECTIVE 1		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **POWER CONVERTERS**		
Course Code: **P24MECE144**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	
Credits:**03**		
Prerequisite:		
Basic Electronics, Analog Electronics Circuits, Power Electronics		
Course learning Objectives:		
CLO1: To analyze Power diodes and rectifiers. CLO2: To analyze and design DC to DC converters. CLO3: To analyze DC to AC converters. CLO4: To analyze Switched circuits. CLO5: To analyze AC Voltage Regulators.		
UNIT -1		8 Hours
Power Diodes and Rectifiers: Introduction, Performance Parameters, Single-Phase Full-Wave Rectifiers, Single-Phase Full-Wave Rectifier with *RL* Load, Single-Phase Full-Wave Rectifier with a Highly Inductive Load, Three-Phase Bridge Rectifiers, Three-Phase Bridge Rectifier with *RL* Load, Three-Phase Rectifier with a Highly Inductive Load, Comparisons of Diode Rectifiers, Rectifier Circuit Design, Output Voltage with *LC* Filter.		
Self-Study Content:1. Effects of Source and Load Inductances. 2. Practical Considerations for Selecting Inductors and Capacitors		
Textbook1:3.1-3.5, 3.7-3.12		
Teaching Learning Process: Flip Class		
UNIT 2:		8 Hours
Analysis and design of DC to DC converters: Introduction, Performance Parameters of DC–DC Converters, Principle of Step-Down Operation, Step-Down Converter with *RL* Load, Principle of Step-Up Operation, Step-Up Converter with a Resistive Load, Frequency Limiting Parameters, Converter Classification, Switching-Mode Regulators, Comparison of Regulators.		
Self-Study Content: 1. Multi output Boost Converter, 2. Diode Rectifier-Fed Boost Converter, 3. Design Considerations for Input Filter and Converters		
Textbook1: 5.1 – 5.10		
Teaching Learning Process: PPT		
UNIT 3:		8 Hours
Analysis and design of DC to AC converters: Introduction, Performance Parameters, Principle of Operation, Single-Phase Bridge Inverters, Three-Phase Inverters, Voltage Control of Single-Phase Inverters, Harmonic Reductions, Current-Source Inverters.		
Self-Study Content:1. Boost Inverter 2. Inverter Circuit Design		
Textbook1: 6.1-6.6, 6.8, 6.9		
Teaching Learning Process: PPT		
UNIT 4:		8 Hours
Analysis of switched circuits: **Thyristor:** Introduction, Thyristor Characteristics, Two-Transistor Model of Thyristor.		

Controlled Rectifiers: Introduction, Single-Phase Full Converters, Single-Phase Dual Converters, Three-Phase Dual Converters, Single-Phase Series Converters.

Self-Study Content:1. Thyristor Types
2. Twelve-Pulse Converters
3. Design of Converter Circuits

Textbook1: 9.1-9.3, 10.1,10.2,10.3,10.4,10.7

Teaching Learning Process: Case Study

UNIT 5:	8 Hours

AC Voltage Regulators: Introduction, Performance Parameters of AC Voltage Controllers, Single-Phase Full-Wave Controllers with Resistive Loads, Single-Phase Full-Wave Controllers with Inductive Loads, Three-Phase Full-Wave Controllers, Three-Phase Full-Wave Delta-Connected Controllers, Single-Phase Transformer Connection Changers, Cyclo converters, AC Voltage Controllers with PWM Control, Matrix Converter.

Self-Study Content: 1. Design of AC Voltage-Controller Circuits
2. Effects of Source and Load Inductances

Teaching Learning Process: Case Study

Textbook1: 11.1-11.10

Course Outcomes: At the end of the course students should be able to :

CO1: Analyse the Power diodes and rectifiers.
CO2:Analyze and Design DC to DC converters.
CO3: Analyze and Design the DC to AC converters.
CO4:Analyze the Switched circuits
CO5:Analyze the AC Voltage Regulators

Suggested Learning Resources:

Textbooks:

1.	Title	Author	Year & Edition	Publisher
1.	Power Electronics Devices, Circuits, and Applications	Muhammad H. Rashid	2014. Fourth Edition	Pearson Education Limited

Reference Books:

1.	PowerElectronics:converters,Applicationanddesign’	NedMohan,UndelandandRobbin	2003. Third Edition	JohnWiley
2.	Principles of Electric Machines and PowerElectronics	P.CSen.,	2007 Second Edition,NewDelhi,	JohnWiley

Web links and Video Lectures (e-resources)

1.https://pdfcoffee.com/power-electronics-converters-applications-and-design-third-edition-ned-mowpdf-pdf-free.html
2.https://archive.nptel.ac.in/courses/117/103/117103148/
3.https://archive.nptel.ac.in/courses/108/102/108102157/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study

5. Learn by Doing

PART-B		
Academic year:2024-25	**Semester:**I	**Scheme:**P24
Course Title: **POWER CONVERTERS**		
Course Code: **P24MECE144**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P) 3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 03	
Credits:03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Analyse the Power diodes and rectifiers.	L2	PO2,PO5
CO2: Analyze and Design DC to DC converters.	L2, L3	PO2, PO5
CO3: Analyze and Design the DC to AC converters.	L2,L3	PO2, PO4
CO4: Analyze the Switched circuits	L2	PO2, PO3
CO5: Analyze the AC Voltage Regulators	L2	PO2, PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1		2			2		
CO2		2			2		
CO3		2		2			
CO4		2	2				
CO5		2		2			

PROFESSIONAL ELECTIVE 2		
PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED EMBEDDED SYSTEMS**		
Course Code: **P24MECE151**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Prerequisite:		
Basic knowledge of digital electronics, Embedded systems concepts, including microcontroller programming and familiarity with C/C++ programming languages.		
Course learning Objectives:		
CLO1: To understand the difference between Embedded Systems and General Computing Systems. CLO2: To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems CLO3: Analysis of a Real Life example on the bonding of Embedded Technology with Human Life CLO4: To understand the difference between Microcontrollers and ARM Cortex processors. CLO5: To learn Programming using assembly and C language, CMSIS for variety of End Applications.		
UNIT -1		8 Hours
Embedded System: Embedded v/s General Computing System, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opt coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems.		
Self-Study Content:1. Explore how Embedded systems perform specific tasks in automotive, medical, and electronics. 2. Study UART, I2C, SPI protocols and SOC design tools.		
Textbook Map:-Text 1: 1.1-1.6,2.1-2.7,3.1-3.2		
Teaching Learning Process: Flipped Classroom/PPT		
UNIT 2:		8 Hours
Hardware Software Co-Design: Embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging.		
Self-Study Content: 1. Learn C, C++, and assembly languages for embedded system development. 2. Discuss the tools are available for the Embedded system design		
Textbook Map: Text 1: 9.1-9.2,12.1,13.1-13.4		
Teaching Learning Process: Quiz/PPT		
UNIT 3:		8 Hours
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM CortexM3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence.		
Self-Study Content: 1. Compare ARM 32-bit architecture with other microcontroller architectures.		

2. Prepare the report on in today electronics industry.	
Textbook Map: Text 2:1.1-1.5,2.1-2.9,3.1-3.7	
Teaching Learning Process: Think Pair share- peer teaching/PPT	
UNIT 4:	8 Hours
InstructionSets: Assemblybasics,Instructionlistanddescription,usefulinstructions,MemorySystems,Memorymaps,CortexM3implementationoverview,pipelineandbusinterface,Exceptions,NestedVectorinterruptcontrollerdesign,SystickTimer,Cortex-M3ProgrammingusingassemblyandClanguage,CMSIS.	
Self-Study Content:1. Identify the usage of Memory Systems in real time. 2. Explore programming ARM Cortex-M3 microcontrollers using both assembly and C language.	
Textbook Map: Text 2:4.1-4.4,5.1-5.8,6.1-6.7,7.1-7.6,8.1-8.5,10.1-10.8	
Teaching Learning Process: Seminar/ PPT	
UNIT 5:	8 Hours
Introduction to RISC-V: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization	
Self-Study Content:1. Study how operands are used and processed in RISC-V hardware. 2. Explore how instructions are represented and stored in RISC-V systems.	
Textbook Map: Text 3: 2.1-2.11	
Teaching Learning Process: Seminar/PPT	
Course Outcomes: At the end of the course students should be able to :	
CO1: **Understand** and apply knowledge of electronic circuits to explore the features of the ARM Cortex-M3, and design a real-time system that leverages its processing power, efficient interrupt handling, and power efficiency for performance. CO2: **Demonstrate** the use of a specific firmware design approach in the code design process. CO3: **Develop** the code for ARM Cortex-M3 microcontrollers using both assembly and C language. CO4: **Design** and implement an advanced embedded system that integrates RISC-V processor features using any suitable tool.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Introduction to embedded systems	K.V.Shibu	2009	TMH education Pvt. Ltd
2	The Definitive Guide to the ARM Cortex-M3	Joseph Yiu, Newnes,(Elsevier)	2010	2nd Edition
3	Computer Organization and Design RISC-V Edition	David A.Patterson, John L.Hennessy, Morgan Kaufmann	2018	ISBN: 9780128122761.

Reference Books:				
1.	Embedded systems-A contemporary design tool	James K.Peckol, John Wiley	2008	2nd Edition
Web links and Video Lectures (e-resources)				
1. https://nptel.ac.in/				
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)				
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing				

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **ADVANCED EMBEDDED SYSTEMS**		
Course Code: **P24MECE151**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P): 3 : 0 : 0	SEE Marks:100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam hours:3 Hours	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Understand and apply knowledge of electronic circuits to explore the features of the ARM Cortex-M3, and design a real-time system that leverages its processing power, efficient interrupt handling, and power efficiency for performance.	.L1	PO1
CO2: Demonstrate the use of a specific firmware design approach in the code design process.	L2	PO2
CO3: Develop the code for ARM Cortex-M3 microcontrollers using both assembly and C language.	L5	PO3
CO4: Design and implement an advanced embedded system that integrates RISC-V processor features using any suitable tool	L5	PO4

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3			2				2
CO4				3			2

PART-A		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **ADVANCED WIRELESS COMMUNICATION**		
Course Code: **P24MECE152**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P)= 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Prerequisite:		
Fundamentals of digital communication signal processing, and wireless network.		
Course learning Objectives:		
CLO1: To enable students understand the various aspects of wireless communication CLO2: To understand the concept behind the capacity of channels CLO3: Gain the information on Linear time-invariant Gaussian channels, Capacity off adding channels CLO4: Study uplink and downlink model of AWGN channel, fading channels CLO5: Describe different types of diversity, Understanding concept behind modelling of MIMO		
UNIT -1		8 Hours
Physical modelling for wireless channels, Input/output model of the wireless channel: Free space, Fixed transmit and receive antennas, Free space, moving antenna, Reflecting wall, fixed antenna, Reflecting wall, moving antenna Reflection from a ground plane, Power decay with distance and shadowing, Moving antenna, multiple reflectors, The wireless channel as a linear time-varying system, Baseband equivalent model, discrete time baseband model, Additive white noise		
Self-Study Content: **1**.Understand the input/output channel relationship, including channel impulse response, Doppler effect, and noise impacts.		
Textbook Map: **2.1 to 2.2**		
Teaching Learning Process: Quiz/Seminar/Case Study/PPT		
UNIT 2:		8 Hours
Time and frequency coherence, AWGN channel capacity: Time and frequency coherence: Doppler spread and coherence time, delay spread and coherence bandwidth, Repetition coding, Packing spheres, Capacity-achieving AWGN channel codes, Reliable rate of communication and capacity, Resources of the AWGN channel-Continuous-time AWGN channel, Power and bandwidth, Bandwidth reuse in cellular systems.		
Self-Study Content: **1**.Understand how channel stability impacts signal transmission over time and frequency. **2**. Learn AWGN channel capacity using Shannon's theorem, focusing on the relationship between bandwidth, SNR, and maximum data rate.		
Textbook Map: **2.3, 5.1 to 5.2**		
Teaching Learning Process: Quiz/Seminar/Case Study/PPT		
UNIT 3:		8 Hours
Linear time – invariant Gaussian channels, Capacity of adding channels : Single input multiple output(SIMO) channel, Multiple input single output(MISO) channel, Frequency-selective channel, Slow fading channel, receive diversity, Transmit diversity, Transmit and receive diversity, Time and frequency diversity, Outage for parallel channels, Fast fading channel, Transmitter side information, Frequency-selective fading channels		
Self-Study Content: **1**. Explore linear time-invariant (LTI) Gaussian channels, focusing on how they model stable channels with constant properties over time.		
Textbook Map: **5.3 to 5.4**		

Teaching Learning Process: Quiz/Seminar/Case Study/PPT	
UNIT 4:	8 Hours
Uplink and Downlink AWGN channel, Uplink and Downlink fading channel: Capacity via Successive interference cancellation, Comparison with conventional CDMA, Comparison with orthogonal multiple access, General K-user uplink capacity, Symmetric case: Two capacity achieving schemes, General case: super position coding achieves capacity, Slow fading channel, Fast fading channel, Full channel side information, Channel side information at receiver only, Full channel side information, Frequency selective fading channels.	
Self-Study Content: **1**.What role does power control play in managing uplink and downlink performance in fading environments.	
Textbook Map: **6.1 to 6.5**	
Teaching Learning Process: Quiz/Seminar/Case Study/PPT	
UNIT 5:	8 Hours
Multi user diversity, Physical Modeling of MIMO channels: Multiuser diversity gain, Multiuser versus classical diversity, Fair scheduling and multi user diversity, Channel prediction and feedback, Opportunistic beam forming using dumb antennas ,Multiuser diversity in multi cell systems, Line-of-sight SIMO channel, Line-of-sight MISO channel, Antenna arrays with only a line-of- sight path, Geographically separated antennas, Line-of-sight plus one reflected path, MIMO multipath channel, Angular domain representation of signals, Angular domain representation of MIMO channels, Statistical modeling in the angular domain, Degrees of freedom and diversity, Dependency on antenna spacing.	
Self-Study Content: **1**.Explore physical modeling of MIMO channels to learn how spatial multiplexing and diversity enhance capacity and reliability in wireless systems.	
Teaching Learning Process: Quiz/Seminar/Case Study/PPT	
Textbook Map: **6.6 to 6.7, 7.2 to 7.3**	
Course Outcomes: At the end of the course students should be able to :	
CO1: Apply knowledge of communication systems to understand physical wireless channel models. CO2: Examine the effects of key parameters on the capacity of AWGN, LTI Gaussian, and fading channels. CO3: Develop advanced techniques to accurately model and estimate multiuser channels for effective resource allocation. CO4: Simulating the performance of various uplink and downlink models using existing tools.	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	Fundamentals of Wireless Communications	David Tse, Pramod Viswanath		Cambridge University Press, 2005 ISBN: 978-0-521-84527-4
2	Wireless Communications	Andrea Goldsmith	2nd Edition	Cambridge University Press,2005 ISBN-10 : 9780521704168 ISBN-13 : 978-0521704168

Reference Books:

1.	Wireless Communications:	Theodore Rappaport.	2nd Edition	Pearson Education India ISBN 9332576165, 9789332576162

	Principles and Practice			
2.	Wireless Communication Systems	Ke-Lin Du and M. N. S. Swamy		Cambridge University Press, 2010 ISBN: 0521114039,9780521114035

Web links and Video Lectures (e-resources)

.https://nptel.ac.in/

Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title**: ADVANCED WIRELESS COMMUNICATION**		
Course Code: **P24MECE152**	CIE Marks: 50	CIE Weightage: 50%
Teaching hours/week (L:T:P)= 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy: 40	Exam Hours: 3 Hours	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	**Expected Bloom's Level**	**Program Outcomes**
CO1: Apply knowledge of communication systems to understand physical wireless channel models	L3	PO1
CO2: Examine the effects of key parameters on the capacity of AWGN, LTI Gaussian, and fading channels	L3	PO3
CO3: Develop advanced techniques to accurately model and estimate multiuser channels for effective resource allocation.	L4	PO3
CO4: Simulating the performance of various uplink and downlink models using existing tools.	L5	PO2,3

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2			2				2
CO3		1				1	
CO4		1	1				1

PART-B		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **MULTIMEDIA AND APPLICATIONS**		
Course Code: **P24MECE153**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P)=3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3(Theory)	
Credits: **03**		
Prerequisite:		
Basic knowledge of multimedia including text, image, audio, video including network terminology. Additionally an understanding of different multimedia compression techniques is recommended.		
Course learning Objectives:		
CLO1:Understand different multimedia encoding schemes and principles of compression algorithms CLO2:Apply the encoding techniques for given data. CLO3:Understand the mechanism of audio and video compression techniques and multimedia networks.		
UNIT -1		8 Hours
Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video. **RBT Levels:** L2		
Self-Study Content: Prepare a report of historical representation of multimedia information representation.		
Textbook Map:1.1, 1.2,1.3,1.4,1.5, Ch 2:2.2-2.6		
Teaching Learning Process: Power point presentation with case studies		
UNIT 2:		8 Hours
Text and image compression: Compression principles, Text compression-Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression-GIF, TIFF and JPEG. **RBT Levels:** L3		
Self-Study Content: Understand the decoding of received bit stream.		
Textbook Map: 3.1, 3.2,3.3.5,3.4.1,3.4.2,3.4.5		
Teaching Learning Process: Power point presentation with case studies		
UNIT 3:		8 Hours
Audio and Video Compression: Audio compression– principles, DPCM, ADPCM Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles. **RBT Levels:** L3		
Self-Study Content: Error resilience techniques		
Textbook Map:4.1,4.2,4.3, 4.3.1		
Teaching Learning Process: Power point presentation with seminars		
UNIT 4:		8 Hours
Video Compression Standards:H.261, H.263, MPEG, MPEG1, MPEG2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework. **RBT Levels:**L3		
Self-Study Content: Basics of computer based animation		
Textbook Map:4.3.2,4.3.3,4.3.4,4.3.5,4.3.6 ,4.3.7,4.3.4, 3.6		

Teaching Learning Process:Powerpoint presentation with guest lecture				
UNIT 5:				8 Hours
Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD). **RBT Levels:** L3, L4				
Self-Study Content: Understand general concepts of token rings and FDDI.				
Teaching Learning Process: Power point presentation with group discussion				
Textbook Map:9.1,10.4.2,1.4.3				
Course Outcomes: At the end of the course students should be able to :				
Suggested Learning Resources:				
Textbooks:				
1.	Title	Author	Year & Edition	Publisher
1	Multimedia Communications: Applications, Networks, Protocols and Standards	Fred Halsall,Pearson Education Publishers	2001	ISBN: 97802013981871.
2	Multimedia: Computing, Communications andApplications	Raif Steinmetz, KlaraNahrstedt	2002	
Reference Books:				
1.	Multimedia Communication Systems	K.R.Rao,Zoran S.Bojkovic, DragoradA.Milovanovicm	2004	
2.	Multimedia Networks: Protocols, Design and Applications	Hans. W. Barz, Gregory A. Bassett	2016	ISBN:9781119090137
3.	Multimedia: An Introduction	John Billamil, Louis Molina	2002	
Web links and Video Lectures (e-resources)				
1.https://nptel.ac.in/				
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)				
1. Flip Class 2. Seminar/ poster Presentation 3. Individual Role play/Team Demonstration/ Collaborative Activity 4. Case study 5. Learn by Doing				

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **MULTIMEDIA AND APPLICATIONS**		
Course Code: **P24MECE153**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P)=3:0:0	SEE Marks:100	SEE Weightage:50%
Teaching hours of Pedagogy:40	Exam Hours: 3(Theory)	
Credits: **03**		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Compare encoding schemes, multimedia techniques and multimedia communication models.	L2	PO2
CO2: Illustrate the working of encoding schemes and multimedia algorithms.	L2	PO2
CO3: Design a subsystem and/or multimedia framework for given requirements.	L4	PO2
CO4: Analyse the impact and effectiveness of multimedia technique, routing technique and multimedia network.	L3	PO5

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1		2					1
CO2		2					1
CO3		2					1
CO4					2		1

PART-B		
Academic Year: 2024-25	Semester: I	Scheme: P24
Course Title: **PROCESS CONTROL**		
Course Code: **P24MECE154**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: **03**		
Prerequisite:		
Electronic and Instrumentation, Control System		
Course learning Objectives:		
CLO1: To understand the need of process control, basic principles of various manufacturing processes. CLO2: Apply engineering knowledge to do problem analysis in process control. CLO3: To select the proper controller and apply the tuning rules to achieve optimum performance. CLO4:To understand and interpret the predictive Control, Multivariate Statistical Techniques CLO5: Apply knowledge of process control in Bio systems control design.		
UNIT -1		8 Hours
Introduction to Process Control- Representative Process Control Problems, Illustrative Example—A Blending Process, Classification of Process Control Strategies, A More Complicated Example—A Distillation Column, The Hierarchy of Process Control Activities, An Overview of Control System Design. **Theoretical Models of Chemical Processes-**The Rationale for Dynamic Process Models, General Modeling Principles, Degrees of Freedom Analysis, Dynamic Models of Representative Processes, Process Dynamics and Mathematical Models		
Self-Study Content: Laplace Transforms of Representative Functions, Solution of Differential Equations by Laplace Transform Techniques, Partial Fraction Expansion		
Textbook Map: 1.1– 1.6, 2.1– 2.5		
Teaching Learning Process: Poster presentation/Quiz/Seminar/Team demonstration		
UNIT 2:		8 Hours
Transfer Function Models- Introduction to Transfer Function Models, Properties of Transfer Functions, Linearization of Nonlinear Models **Dynamic Behaviour of First-Order and Second-Order Processes-** Standard Process Inputs, Response of First-Order Processes, Response of Integrating Processes, Response of Second-Order Processes		
Self-Study Content: Dynamic Behaviour and Stability of Closed-Loop Control Systems, Closed-Loop Transfer Functions, Closed-Loop Responses of Simple Control Systems.		
Textbook Map: 4.1- 4.3, 5.1- 5.4		
Teaching Learning Process: Flip class/Quiz/Seminar/Team demonstration		
UNIT 3:		8 Hours
Dynamic Response Characteristics of More Complicated Processes- Poles and Zeros and Their Effect on Process Response, Processes with Time Delays, Approximation of Higher-Order Transfer Functions, Interacting and Non interacting Processes, State-Space and Transfer Function Matrix Models, Multiple-Input, Multiple-Output (MIMO) Processes. **Development of Empirical Models from Process Data-** Model Development Using Linear or Nonlinear Regression, Fitting First- and Second-Order Models Using Step Tests, Neural Network Models, Development of Discrete-Time Dynamic Models**,** Identifying Discrete-Time Models from Experimental Data.		

Self-Study Content: Performance Criteria for Closed-Loop Systems, Model-Based Design Methods, Controller Tuning Relations, Controllers with Two Degrees of Freedom.	
Textbook Map: 6.1- 6.6, 7.1- 7.5	
Teaching Learning Process: Quiz/Seminar/Team demonstration/One minute paper writing	
UNIT 4:	8 Hours
Feedback Controllers- Introduction**,** Basic Control Modes, Features of PID Controllers, Digital Versions of PID Controllers, Typical Responses of Feedback Control Systems, On–Off Controllers. **Control System Instrumentation-** Sensors, Transmitters, and Transducers, Final Control Elements Accuracy in Instrumentation	
Self-Study Content: Process Safety and Process Control, Layers of Protection, Alarm Management, Abnormal Event Detection, Risk Assessment	
Textbook Map: 8.1- 8.6. 9.1- 9.3	
Teaching Learning Process: Think pair share/One minute paper writing/ Quiz/Seminar	
UNIT 5:	8 Hours
Model Predictive Control - Overview of Model Predictive Control, Predictions for SISO Models**,** Predictions for MIMO Models **Process Monitoring-**Traditional Monitoring Techniques, Quality Control Charts, Multivariate Statistical Techniques **Bio systems Control Design-** Process Modelling and Control in Pharmaceutical Operations, Process Modelling and Control for Drug Delivery	
Self-Study Content: Model Predictive Control Calculations, Set-Point Calculations, Selection of Design and Tuning Parameters, Control Performance Monitoring	
Teaching Learning Process: One minute paper writing/ Quiz/Seminar/Team demonstration	
Textbook Map: 20.1, 20.2, 20.3, 21.1, 21.2, 21.4, 23.1, 23.2.	
Course Outcomes: At the end of the course students should be able to :	
Suggested Learning Resources:	
Textbooks:	

1.	Title	Author	Year & Edition	Publisher
1	"Process Dynamics and Control"	D. E. Seborg, T.F. Edgar, D. A. Mellichamp	2004, Fourth Edition	Wiley
2	"Chemical Process Control An Introduction to Theory and Practice"	G. Stephanopolous	August 2000.	Prentice Hall India,
Reference Books:				
1.	"Process Control Instrumentation Technology"	C.D. Johnson,	2014	Prentice Hall India.
2.	"Process Control Systems Application Design and Adjustment"	F.G. Shinskey	3rd edition,	McGraw Hill International, 6. D.

Web links and Video Lectures (e-resources)
Active Based Learning (Suggested Activity in Class)/ Practical Based Learning (Example)

1. Flip Class
2. Seminar/ poster Presentation
3. Individual Role play/Team Demonstration/ Collaborative Activity
4. Case study
5. Learn by Doing

PART-B		
Academic year:2024-25	Semester: I	Scheme:P24
Course Title: **PROCESS CONTROL**		
Course Code: **P24MECE154**	CIE Marks:50	CIE Weightage:50%
Teaching hours/week (L:T:P): 3:0:0	SEE Marks: 100	SEE Weightage: 50%
Teaching hours of Pedagogy:40	Exam Hours: 3 hours	
Credits: 03		
Name of the Course Coordinator: [team designing the course]		

Course Outcomes	Expected Bloom's Level	Program Outcomes
CO1: Apply knowledge to implement process control systems using theoretical and mathematical models.	**L3**	**PO1**
CO2: Analyze empirical models from process data to predict chemical process dynamics and design control strategies.	**L4**	**PO2**
CO3: Design and implement feedback controllers, select instrumentation, and tune parameters for optimal performance.	**L6**	**PO1**
CO4: Develop process control systems with sensors, actuators, and optimization for efficient operation.	**L6**	**PO4**

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	2						2
CO2		2					2
CO3	2						
CO4				2			

VLSI DESIGN LAB			
Course Code	**P24MECEL16**	CIE Marks	50
Teaching Hours/Week(L:P:T/SDA)	0:1:1	SEE Marks	50
Credits	02	Exam Hours	03(Practical)

Course Objectives:

- To Familiarize with the ASIC flow and cadence tool suite
- To Debug and develop RTL code
- To perform functional verification, Logical equivalence check(LEC), Timing and power analysis.
- To Develop embedded code for the given requirements
- To perform testing and verification of multithread application.

Sl.No.	Experiments
	Part–A **VLSI Digital Design**
1	Write Verilog Code for the following circuits and their Test Bench for verification, ➢ An inverter, Buffer and Transmission gate ➢ Basic/Universal gates ➢ Flip flop -RS, D, JK, MS, T
2	Write Verilog code for the following circuits and their Test Bench for verification ➢ Carry Ripple Adder ➢ Carry Look Ahead adder ➢ Carry Skip Adder
3	Design the following circuits using ASIC Digital Design flow and Write a Verilog Code for 8-bit Booth Multiplication (Radix-4)
4	Design the following circuits using ASIC Digital Design flow and Write Verilog code for 4/8-bit Magnitude Comparator, Parity Generator,
5	Design the following circuits using ASIC Digital Design flow and Write Verilog code for 4/8-bit, LFSR, Universal Shift Register
6	Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
	Part–B **VLSI Analog Design (Upto Post Layout Simulation)**
7	Design single stage differential amplifier
8	Design a simple 4/8-bit ADC converter
9	Design an op-amp with given specification* using differential amplifier Common source amplifier in library**

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

1. **Develop** RTL code/Embedded code for given requirement
2. **Analyze** the given RTL/Embedded code.
3. **Debug** the given RTL/Embedded code
4. **Design** and **simulate** a module/system for given requirements

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is 50 Marks.

The split-up of CIE marks for record/ journal and test are in the ratio 60:40.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The test marks is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours

Suggested Learning Resources:

- **"Introduction to Embedded Systems",** Shibu K V, TMH Education Pvt Ltd, Second reprint, 2010, ISBN(13): 978-0-07-014589-4.
- **"Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology: Circuit Design, and Process Technology"** Luciano Lavagno, Igor L. Markov, Grant Martin, Louis K. Scheffer, CRC Press, ISBN-10: 0-8493-7924-5, ISBN-13: 978-0-8493-7924-6, 2006**..**
- **"Digital VLSI Design (RTL to GDS)"**Dr. Adam Teman , Emerging nano scaled Integrated Circuits and Systems (En ICS) Labs Faculty of Engineering, Bar-Ilan University

COURSE ARTICUALTION MATRIX							
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PSO1**	**PSO2**
CO1	3					3	
CO2		2					2
CO3	2					2	
CO4			3				3