SYLLABUS
Academic Year 2018-19

Master of Technology
In
VLSI Design and Embedded Systems

Department of Electronics and Communication Engineering
P.E.S. College of Engineering
Mandya- 571401, Karnataka
(An Autonomous Institution under VTU, Belagavi)
P.E.S COLLEGE OF ENGINEERING, MANDYA

P.E.S COLLEGE OF ENGINEERING, MANDYA-571401
(KARNATAKA)
(An Autonomous Institution under VTU, Belagavi)

Vision

PESCE shall be a leading institution imparting quality engineering and management education developing creative and socially responsible professionals.

Mission

- Provide state of the art infrastructure, motivate the faculty to be proficient in their field of specialization and adopt best teaching-learning practices.
- Impart engineering and managerial skills through competent and committed faculty using outcome based educational curriculum.
- Inculcate professional ethics, leadership qualities and entrepreneurial skills to meet the societal needs.
- Promote research, product development and industry-institution interaction.
About the department:

The department of Electronics and Communication Engineering was incepted in the year 1967 with an undergraduate program in Electronics and Communication Engineering. Initially program had an intake of 60 students and presently 150 students graduate every year. The long journey of 50 years has seen satisfactory contributions to the society, nation and world. The alumni of this department has strong global presence making their alma mater proud in every sector they represent.

Department has started its PG program in the year 2012 in the specialization of VLSI design and Embedded systems. Equipped with qualified and dedicated faculty department has focus on VLSI design, Embedded systems and Image processing. The quality of teaching and training has yielded high growth rate of placement at various organizations. Large number of candidates pursuing research programs (M.Sc/Ph D) is a true testimonial to the research potential of the department.

Vision

The department of E & C would endeavour to create a pool of Engineers who would be extremely competent technically, ethically strong also fulfil their obligation in terms of social responsibility.

Mission

- **M1:** Adopt the best pedagogical methods and provide the best facility, infrastructure and an ambience conducive to imbibe technical knowledge and practicing ethics.
- **M2:** Group and individual exercises to inculcate habit of analytical and strategic thinking to help the students to develop creative thinking and instil team skills
- **M3:** MoUs and Sponsored projects with industry and R & D organizations for collaborative learning
- **M4:** Enabling and encouraging students for continuing education and moulding them for life-long learning process
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(A) Programme Learning Objectives (PLOs)
M.Tech in VLSI Design and Embedded system during two years term, aims to
1. Provide the students with strong fundamental and advanced knowledge in VLSI Design and Embedded system with an emphasis to solve engineering problems.
2. Train the students in VLSI and Embedded system design tools and make them fit for the industries.
3. Inculcate in students the professional and ethical attitude, effective communication skills, team spirit and nurture them as leaders.
4. Provide teaching skills and inculcate spirit of research.
5. Motivate to continue education leading to doctoral degree and choose research as career option.

(B) Programme Outcomes (POs):
The Master of Technology Programme in Electronics and Communication Engineering [M.Tech in VLSI Design and Embedded system] must demonstrate that it’s Post graduates have
1. An ability to apply knowledge gained out of this program to develop products and solutions in the area of VLSI design and Embedded Systems.
2. An understanding of professional and ethical responsibilities at national and international levels.
3. An ability to effectively communicate both written and oral on social and technical problems at national and global scenarios.
4. An ability to engage in independent and lifelong learning in the broad context of technological change.
5. Ability to carry-out independent research.

A total of 88 credits for 2 years M.Tech programme

Credit pattern

Core Courses:- I Semester 12 credits
   II Semester 12 credits
Total credits for core courses is 24 credits

Elective Course: - I Semester 08 credits
   II Semester 08 credits
Total credits for Elective courses is 16 credits

Self Study course: - 04 credits
Seminar: - 04 credits
Lab: - 04 credits
Industrial Training: - 04 credits
Pedagogy Training: - 04 credits
Project work:- 28 credits A total of 88 credits for 2 years M.Tech programme
M.Tech in VLSI Design and Embedded System Program  
(OBE) for the  
Academic year 2018-20

**Scheme of Teaching and Examination**

**First semester**

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Sub. Code</th>
<th>Subject</th>
<th>Teaching Dept.</th>
<th>Hrs./Week</th>
<th>Total Credits</th>
<th>Marks Allocated</th>
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<tr>
<td>1.</td>
<td>P18MECE11</td>
<td>CMOS VLSI Design</td>
<td>EC</td>
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**Elective – I**

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<td>P18MECE141</td>
<td>VLSI Technology</td>
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<td>2.</td>
<td>P18MECE142</td>
<td>Digital system design using Verilog</td>
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**Elective – II**

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<td>3.</td>
<td>P18MECE151</td>
<td>ASIC Design</td>
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<td>4.</td>
<td>P18MECE152</td>
<td>Multicore Architecture</td>
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<td>P18MECE21</td>
<td>Design of Analog and Mixed Mode VLSI Circuits</td>
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<td>Low Power VLSI Design</td>
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<td>P18MECE23</td>
<td>Real time Systems</td>
<td>EC</td>
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<td>P18MECE241</td>
<td>ARM Processor</td>
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<td>2</td>
<td>P18MECE242</td>
<td>Embedded System Design with FPGA</td>
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<td>3</td>
<td>P18MECE251</td>
<td>System Verilog</td>
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<td>4</td>
<td>P18MECE252</td>
<td>Design Of VLSI System</td>
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### Third semester

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<td>2.</td>
<td>P18MHSM32</td>
<td>Pedagogy/Research Methodology</td>
<td>HS&amp;M</td>
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<td>P18MECE33</td>
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<td>P18MECE34</td>
<td>Project –Phase – I</td>
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<tr>
<td>1.</td>
<td>P18MECE41</td>
<td>Project –Phase-III</td>
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<td>2.</td>
<td>P18MECE42</td>
<td>Project –Phase-IV(Thesis Evaluation)</td>
<td>EC</td>
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<td>3.</td>
<td>P18MECE43</td>
<td>Project –Phase-V(Viva-Voce)</td>
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<td>4.</td>
<td>P18MECE44</td>
<td>Term Paper</td>
<td>EC</td>
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</table>
Category of Courses:

1. **Core Courses**: The Core courses constitute the core of the programme of study. Core courses are to be compulsorily studied by a student and are mandatory to complete them to fulfill the requirements of a programme.

2. **Electives**: Elective courses offer a choice of advanced or specialized courses related to the programme of study. They enable students to specialize in a domain of interest or tune their learning to suit career needs and current trends.

3. **Laboratories**: The Laboratories are evaluated for 100 marks which includes CIE: 50 marks & SEE: 50 marks. The assessment of CIE is done with execution of lab programs & report submission. The final SEE assessment is done with the conduction of exam and Viva-Voce.

4. **Self-Study Course**: The Self-Study Course shall consist of five units with lab component and he/she must be able to demonstrate the knowledge gained by the candidates. The course content must be tailor made by the department to suit their requirements. The Self-Study Course shall be assessed for 100 marks. The evaluation is based on the lab report submission/ assignment/ viva-voce as CIE 50 marks and SEE for 50 marks.

5. **Industrial training**: The Industrial training shall be completed during the period specified in the Scheme of Teaching and Examination.
   
   I. The industrial training can be carried out in any industry/ R & D Organization/ Research / Institute/ Educational institute of repute / Internshala (AICTE MoU Internship).
   
   II. The Department/college shall nominate staff member/s to facilitate, guide and supervise students under Industrial training.
   
   III. The Internal Guide has to visit place of Industrial training at least once during the student’s Industrial training.
   
   IV. The students shall report the progress of the Industrial training to the guide in regular intervals and seek his/her advice.
   
   V. After the completion of Industrial training, students shall submit a report with completion and attendance certificates to the Head of the Department with the approval of both internal and external guides.
   
   VI. A report on Industrial Training is to be submitted by the student. The report has to be evaluated by Industrial guide and Institute guide for CIE of 50 marks (industry and supervisor evaluation average marks for 50 each). The student must give seminar based on Industrial Training before a committee constituted by the department for remaining CIE of 50 marks.
   
   VII. **Failing to undergo Industrial Training**: Industrial Training is one of the head of passing. Completion of Industrial Training is mandatory. If any student fails to undergo /complete the Industrial Training, he/she shall be considered as failed in that Course. The reappearance shall be considered as an attempt.
VIII. Eight weeks of compulsory Industrial Training to be undergone by the students during their III semester.

6. **Pedagogy/Research methodology:** Pedagogy/Research methodology is CIE with objective type of question for evaluation.

7. **Seminar:** The seminar shall be of 100 marks CIE. It is based on the current topics presentation along with a report submission for evaluation each of 50 marks.

8. **Project Work:** The Project Work carries 28 credits and spreads over TWO semesters, i.e. during III and IV semesters. Project work Phase-1, 2 & 3 to be awarded by the Department committee constituted for the purpose.
   
   I. The Project Phase-I evaluation shall be of 100 marks CIE. It is based on Report Submission consisting of Title, Introduction, Literature Survey, Summary of Literature Survey, Objectives and Methodology (50 Marks) and Presentation (50 marks) each.
   
   II. The Project Phase-II evaluation shall be of 100 marks CIE. It is based on Report Submission consisting of Experimentation, Theoretical analysis approach and results (if completed as a stage work) and Presentation for 50 marks each.
   
   III. The Project Phase-III evaluation shall be of 100 marks CIE. It is based on Thesis manuscript and presentation for 50 marks each (work completion report).
   
   IV. The Project Phase-IV evaluation shall be of 100 marks CIE. It is based on the evaluation done separately by internal and external examiners and average marks of the two examiner shall be consider as final marks.
   
   V. The Project Phase-V evaluation shall be of 100 marks SEE. It is based on Thesis presentation and project viva voce has to be conducted jointly by internal and external examiner for a total of 100 marks SEE.

9. **Term Paper:** The term paper is purely based on the project work he/she chooses.
   
   I. The Term paper shall be for 100 marks CIE only. It has to be evaluated by the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate.
   
   II. The term paper evaluation is based on the publication of an article in peer reviewed conference/journal (national/ international) and quality of the journal. If the term paper is not published by the candidate or the same is communicated for publication at the end of his/ her tenure, then the committee formed by HOD consisting of PG coordinator, guide and subject expert internal/ external for each candidate will asses for the award of credit.
Course Content

FIRST SEMESTER

Course Code: P18MECE11  Semester : I  (L:T:P:H: 4:0:0:4)

Course Title : CMOS VLSI DESIGN

Contact Period : Lecture :52 Hr, Exam: 3Hr  Weightage :CIE:50% SEE:50%

Prerequisites:
The student should have undergone the course on basic CMOS VLSI Design.

Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the basic knowledge of MOSFETs.
2. Explain the MOS Transistor threshold voltage equation.
3. Describe the second order effects.
4. Provides the knowledge of lambda based design rule and process technology
5. Outline the concepts of Basics of Digital CMOS Design.
6. Discuss the concepts of clocking in digital CMOS design
7. Describe the different types of semiconductor memories.

Course Content

UNIT I:

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics.

The CMOS Inverter: Analysis and Design: Basic Circuit and DC Operation, Inverter Switching Characteristics, Output Capacitance, Inverter Design. 10 Hrs

UNIT II:

Combinational MOS Logic Circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate.

MOS Inverters Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter. 10Hrs

UNIT III:

Voltage boot strapping synchronous dynamic circuit’s techniques, Dynamic CMOS circuit techniques.

**Semiconductor Memories:** Introduction, Read-Only Memory (ROM) Circuits, Static Read-Write Memory (SRAM) Circuits, Dynamic Read-Write Memory (DRAM) Circuit. 11Hrs

**UNIT IV:**

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS/SOS technology, CMOS/bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements. 10Hrs

**UNIT V:**

CMOS Process Technology: Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays, driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits. 11Hrs

**TEXT BOOKS**


**REFERENCE**


**Course Outcome (CO)**

The student is able to

1. Apply the knowledge of the basic VLSI circuit to understand the concept of MOSFET, CMOS circuit, digital circuits.
2. Analyze the MOSFET and CMOS circuits.
3. Analyze the CMOS process technology and semiconductor memories.
4. Analyze and design the inverter for different types of load.
5. Design the CMOS circuits using lambda based rule.
Course Code: P18MECE12 | Semester : I | (L:T:P:H: 4:0:0:4)

Course Title : Advanced Embedded systems

Contact Period : Lecture :52 Hr, Exam: 3Hr | Weightage : CIE:50% SEE:50%

Prerequisites:
The student should have undergone the course on basic embedded systems and microcontrollers architecture and programming.

Course Learning Objectives (CLOs)
At the end of the course the students should be able to:
1. Understand basic components of embedded systems and its characteristic attributes
2. Partitioning design into Hardware and Software
3. Analyze embedded design problem
4. Use EDA tools and Firmware design tools
5. Understand major issues with RTOS
6. Write software for the embedded system using Embedded C
7. Choose proper IDE for the design and follow the recent trends in the embedded system design.

Course Content

UNIT I:
Characteristics and Quality Attributes of Embedded Systems: Characteristics of an embedded system, Quality attributes of embedded systems.

Embedded System- Application and Domain Specific: Consumer (Washing Machine), Automotive

UNIT II:
Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

Electronic Design Automation (EDA) Tools: How to use OrCAD tool, schematic design using OrCAD Capture CIS.

UNIT III:
Real-Time Operating System (RTOS) based Embedded System Design:
Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and
Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS (Only conceptual understanding, no programming implementation). **11 Hrs**

**UNIT IV:**

Programming in Embedded C: Programming in Embedded C, C vs Embedded C, Compiler vs Cross Compiler, Using C in Embedded C. **10 Hrs**

**UNIT V:**

The Embedded System Development Environment: The Integrated Development Environment (keil microvision 3 for illustration only), Types of Files Generated on Cross compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.


**TEXT BOOK:**


**REFERENCE**


**Course Outcome (CO)**

The student should be able to

1. Analyze Embedded systems for its requirement and specifications
2. Design simple Embedded systems
3. Analyze different issues of RTOS
4. Discuss recent trend in the Design of Embedded systems
5. Develop software for embedded systems using Embedded C.
Course Code: P18MECE13 | Semester : I | (L:T:P:H: 4:0:0:4)
Course Title : SOC design
Contact Period : Lecture :52 Hr, Exam:3Hr | Weightage :CIE:50% SEE:50%

**Course Learning Objectives (CLOs)**

At the end of the course the students should be able to:

1. Compare the performance, advantages, and disadvantages of system on board, system on chip, and system in package.
2. Provide the overview of embedded processors with different architectures and embedded memories with scratchpad and cache concepts.
3. Describe the hardware accelerators for graphics and image processing as well as DMA controller and USB controller.
4. Outline the interfacing procedure to connect D/A converter with the microcomputer.
5. Focus on the vital issues of ESL design flow for MPSoCs.

**Course Content**

**UNIT I**

Comparison between System-on-Board, System-on-Chip, and System-in-Package. Motivation for SOC Design Review of Moore’s law, benefits of system-on-chip integration in terms of cost, power, and performance, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse, CMOS scaling. **11 Hrs**

**UNIT II**

**Embedded Processors** – microprocessors, microcontrollers, DSP and their selection criteria. Review of RISC and CISC instruction sets, Von-Neumann and Harvard architectures, and interrupt architectures.

**Embedded Memories** – scratchpad memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence. **10 Hrs**

**UNIT III**

**Hardware Accelerators in an SOC** – comparison on hardware accelerators and general-purpose CPU. Accelerators for graphics and image processing. Typical peripherals in an SoC – DMA controller, USB controller.

11 Hrs

UNIT IV

Mixed Signal and RF components in a SoC. Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits.  

10 Hrs

UNIT V

SoC Design Flow. IP design, verification and integration, hardware-software codesign, power management problems, and packaging related problems.  

10 Hrs

TEXT BOOKS


REFERENCES

3. Gray Yeap ”Practical low power Digital design”
4. Kai Hwang,”Advanced computer architecture :parallelism, scalability ,programmability”

Course Outcome (CO)

The student is able to
1. Apply the best design practices to achieve the minituration at optimized cost -(PO1,L3)
2. Analyze with neat sketches the two mechanisms of data programming and erasing the flash memory cell -(PO2,L4)
3. Apply the concepts of CPU accelerators to design systems using many processors. (PO1,L3)
4. Compare the three types of physical structures of shared bus implementation -(PO2,L4)
5. Analyze the Hartley image reject receiver graphically -(PO1,L3)
6. Apply the concepts of voltage control for the Adoptive performance management -(PO1,L3)
ELECTIVE I

Course Code: P18MECE141  |  Semester : I  |  (L:T:P:H: 4:0:0:4)
Course Title : VLSI Technology
Contact Period : Lecture :52 Hr, Exam:3Hr  |  Weightage :CIE:50%SEE:50%

Course Learning Objectives (CLO): 

At the end of the course the students should be able to:

1. Provide the overview of crystal growth technique and thin film technologies.
2. Explain the different lithographic process, plasma formation and etching techniques.
3. Describe the deposition process of polysilicon, oxide, nitride and other materials.
4. Highlight the ion implantation techniques with shallow and deep profiles.
5. Discuss the metallization process and vlsi nmos and pmos fabrication processes.
6. Provide the steps of IC memory fabrication technology and packaging schemes.

Course Content

UNIT I:

Epitaxy: Introduction, Vapour-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation. 10 Hrs

UNIT II:


UNIT III:
Dielectric and Polysilicon Film Deposition: Introduction, Deposition Processes, Polysilicon, Silicon Dioxide, Silicon Nitride, Plasma-Assisted Depositions, Other Materials.

UNIT IV:


VLSI Process Integration: Introduction, Fundamental Considerations for IC Processing, NMOS IC technology, CMOS IC Technology

UNIT V:

MOS Memory IC Technology, Bipolar IC Technology, IC Fabrication.

Packaging of VLSI Devices: Introduction, Package Types, Packaging Design Considerations.

TEXT BOOK


REFERENCE


Course Outcome (CO)

The student is able to

1. Explain wet cleaning and dry cleaning of silicon wafers.
2. Describe optical lithography, electron lithography, X-ray Lithography, Ion Lithography.
3. Discuss the Polysilicon, Silicon Dioxide and Silicon Nitride depositions as well as Plasma-Assisted Depositions.
4. Outline the Metallization Problems and solutions.
5. Describe the VLSI Process Integration and Important Considerations for IC Processing.
Course Code: P18MECE142  Semester : I  (L:T:P:H: 4:0:0:4)

Course Title : Digital System Design Using Verilog

Contact Period : Lecture :52 Hr, Exam:3Hr  Weightage :CIE:50% SEE:50%

Course Learning Objectives (CLOs)

The students should be able to:

1. Understand the concepts of Real world circuits, Models and Design methodology
2. Thoroughly discuss the Combinational Circuits and its Verification.
3. Develop the verilog coding for any applications.
4. Implement the design of any systems like Memories, interconnect etc
5. Design and develop the processor basics and I/O interfacing.

Course Content

UNIT I
Combinational Basics: Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.  11 Hrs

UNIT II
Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers.
Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.  11 Hrs

UNIT III
Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.  10 Hrs

UNIT IV
Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.  10 Hrs

UNIT V
Accelerators: Concepts, case study, Verification of accelerators.
Design Methodology: Design flow, Design optimization, Design for test. 10 Hrs

TEXT BOOK

REFERENCE

Course Outcomes (CO)
The student should be able to

1. Analyze the knowledge of Digital Systems and Embedded Systems.
2. Describe the concepts of Combinational Circuits and its Verification.
3. Develop the verilog code for any applications.
4. Design any combinational circuits and Sequential Circuits.
5. Design and develop the verilog, stimulus for Memories, processor basics and I/O interfacing.
ELECTIVE II

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<th>Semester : I</th>
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<tbody>
<tr>
<td>Course Title : ASIC Design</td>
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<td>Contact Period : Lecture :52 Hr, Exam: 3Hr</td>
<td>Weightage :CIE:50% SEE:50%</td>
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</tbody>
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Course Learning Objectives (CLOs)

This course aims to:

1. Provide the knowledge of ASIC Design Flow.
2. Cover Fundamentals of Full custom, Semi custom and standard cell based design.
3. Explain the low-level design entry.
5. Describe the various concepts of floor planning and placement and routing and partitioning methods.

Course Content

UNIT I

**Introduction:** Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries. **10 Hrs**

UNIT II

**Data Logic Cells:** Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers  
**ASIC Library Design:** Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design. **10 Hrs**

UNIT III

**Low-Level Design Entry:** Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC’S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation. **10 Hrs**

UNIT IV

**Programmable ASIC:** programmable ASIC logic cell, ASIC I/O cell  
**A Brief Introduction to Low Level Design Language:** an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation. **11 Hrs**
UNIT V

TEXT BOOKS

REFERENCE

Course Outcomes (CO)
The student should be able to:
1. Select the type of design flow for any given system.
2. Design systems using cell libraries.
3. Develop systems with Hierarchical design flow.
4. Estimate the various parameters of an ASIC.
Course Code: P18 MECE152  Semester : I  (L:T:P:H: 4:0:0:4)

Course Title : Multicore Architecture

Contact Period : Lecture :52 Hr, Exam:3Hr  Weightage :CIE:50% SEE:50%

Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Provide the knowledge of Multi–core Architecture and System Overview of Threading.
2. Cover Fundamental Concepts of Parallel Programming and its Constructs.
3. Describe in detail the concepts of Threading APIs.
4. Explain the different aspects of OpenMP.
5. Provide Solutions to Common Parallel Programming Problems.

Course Content

UNIT I


Text: Chapters 1 and 2  11 Hrs

UNIT II

Fundamental Concepts of Parallel Programming: Designing for Threads, Task Decomposition, Data Decomposition, Data Flow Decomposition, Implications of Different Decompositions, and Challenges You will Face, Parallel Programming Patterns.

A Motivating Problem: Error Diffusion, Analysis of the Error Diffusion Algorithm.

An Alternate Approach: Parallel Error Diffusion, Other Alternatives.


Text: Chapters 3 and 4  11 Hrs
UNIT III

**Threading APIs:** Threading APIs for Microsoft Windows, Win32/MFC Thread APIs, Threading APIs for Microsoft Dot–NET Framework, Creating Threads, Managing Threads, Thread Pools, Thread Synchronization, POSIX Threads, Creating Threads, Managing Threads, Thread Synchronization, Signaling, Compilation and Linking.

Text: Chapter 5

10 Hrs

UNIT IV


Text: Chapter 6

10 Hrs

UNIT V


Text: Chapter 7

10 Hrs

TEXT BOOK


REFERENCE BOOKS:


Course outcome (CO)
The student is able to
1. Apply the knowledge of parallel programming to solve the design problems.
2. Analyze the dataflow among different cores of the CPU.
3. Design multi core processor system using threads, shared memory, data races, deadlocks and live locks.
4. Develop the architectures and the related algorithms to implement in real systems.
Course Code: P18MECEL16  
Semester : I  
(L:T:P:H: 0:0:4:4)

<table>
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<td>Weightage : CIE:50% SEE:50%</td>
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**Course Learning Objectives (CLOs)**

After learning these course, the student is able to
1. Understand the basic knowledge of how to use EDA Tool for Embedded Hardware Design and for PCB design.
2. Analyze the layout design tool, component placement, routings and design rule checking.
3. Design and Verify an inverter, Buffer, Transmission gate and Basic/universal gates using verilog code.
4. Design and Verify a testing program for specified conditions using multithread application.
5. Design a POSIX based message queue for communicating between two tasks as per the requirements specified

**Course Content**

I. Advanced Embedded Systems

1. Use any EDA (Electronic Design Automation) tool to learn the Embedded Hardware Design and for PCB design.
2. Familiarize the different entities for the circuit diagram design.
3. Familiarize with the layout design tool, building blocks, component placement, routings, design rule checking for the following.
   a. Basic RC Circuit  
   b. Half Wave Rectifier  
   c. Inverting Amplifier  
   d. Half Adder  
   e. Full Wave Rectifier using SCR  
   f. Oscillator Circuit  
   g. Characteristics of BJT in Common Base Configuration  
4. Design an embedded system using microcontroller and verify its operation. (use any EDA tool)

II. Embedded Programming Concepts (RTOS)

1. Create ‘n’ number of child threads. Each thread prints the message “I’m in thread number” and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
2. Implement the multithread application satisfying the following:
   i. Two child threads are created with normal priority.
   ii. Thread 1 receives and prints its priority and sleeps for 50 ms and then quits.
   iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits.
   iv. The main thread waits for the child thread to complete its job and quits.
3. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism.
4. Test the program below using multithread application.
   i. The main thread creates a child thread with default stack size and name ‘Child_Thread’.
   ii. The main thread sends user defined messages and the message ‘WM_QUIT’ randomly to the
       child thread.
   iii. The child thread processes the message posted by the main thread and quits when it receives the
       ‘WM_QUIT’ message.
   iv. The main thread checks the termination of the child thread and quits when the child thread
       complete its execution.
   v. The main thread continues sending the random messages to the child thread till the ‘WM_QUIT’
       message is sent to child thread.
   vi. The messaging mechanism between the main thread and child thread is synchronous.

5. Test the program application for creating an anonymous pipe with 512 bytes of size and pass the ‘Read
   Handle’ of the pipe to a second process using memory mapped object. The first process writes a message
   ‘Hi from Pipe Server’. The 2nd process reads the data written by the pipe server to the pipe and displays it
   on the console. Use event object for indicating the availability of data on the pipe and mutex objects for
   synchronizing the access in the pipe.

6. Create a POSIX based message queue for communicating between two tasks as per the requirements
   given below:-
   i. Use a named message queue with name ‘MyQueue’.
   ii. Create two tasks (Task1 & Task2) with stack size 4000 & priorities 99 & 100 respectively.
   iii. Task1 creates the specified message queue as Read Write and reads the message present, if any,
       from the message queue and prints it on the console.
   iv. Task2 open the message queue and posts the message ‘Hi from Task2’. Handle all possible error
       scenarios appropriately.

Course Outcome
The student should be able to

1. Apply the basic knowledge of how to use EDA Tool for Embedded Hardware Design and
   for PCB design.
2. Analyze the layout design tool, component placement, routings and design rule checking.
3. Develop the multithread application code satisfying the specific functions using Linux.
4. Design a testing program for creating an anonymous pipe with given conditions
5. Design and develop a POSIX based message queue for communicating between two
   tasks as per the requirements specified
SECOND SEMESTER

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<th>Semester : II</th>
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<tr>
<td>Course Title : Design of Analog and Mixed Mode VLSI Circuits</td>
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<td>Contact Period : Lecture :52 Hr, Exam:3Hr</td>
<td>Weightage :CIE:50%SEE:50%</td>
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Course Learning Objectives (CLOs)

At the end of the course the students should be able to:

1. Analyze the analog CMOS VLSI circuits.
2. Develop the small signal hybrid MOS device model starting from the device physics.
3. Write down the equivalent circuits for different amplifier and oscillator MOS circuits.
4. Derive the mathematical expressions for small signal voltage gain, output resistance for different configurations of amplifier circuits.
5. Explain the design and working of band gap references, op-amps.
6. Discuss the operation of switched capacitor circuits, amplifiers and integrators
7. Describe the circuits of ring oscillators, LC oscillators, Voltage controlled oscillators, Phase locked loop and delay lock loops.

Course Content

UNIT I

Basic MOS Device Physics: second order effects, MOS device models.
Single stage Amplifier: CS stage with resistive load, diode - connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models. 11Hrs

UNIT II

Differential Amplifiers: Basic differential pair, common mode response, Differential pair with MOS loads, Gilbert cell.
Passive and active Current mirrors: Basic current mirrors, Cascade mirrors, active current mirrors. 11Hrs

UNIT III

Operational Amplifiers: Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR.
Band gap references, supply-independent biasing, temperature independent references, PTAT current generation, constant gm biasing. 10Hrs
UNIT IV

Switched capacitor circuits, general considerations, sampling switches, switched – capacitor amplifiers, switched – capacitor integrator, Oscillators, general considerations, Ring Oscillators, LC Oscillators, Voltage controlled oscillators, 10Hrs

UNIT V

Phase locked loops (PLL): Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops, applications 10Hrs

TEXT BOOKS:

Course outcome (CO):

The student is able to

1. Apply the concepts of device physics of MOSFETs to construct the small signal Hybrid circuit model for MOSFETs. (PO1,L3)
2. Analyze qualitatively and quantitatively the differential amplifier circuits. (PO2,L4)
3. Construct the band gap references circuits starting from supply independent biasing and temperature independent references. (PO3,L5)
4. Apply the knowledge of switched – capacitor circuits to construct amplifier and integrators. (PO1,L3)
Course Code: P18MECE22  Semester : II  (L:T:P:H: 4:0:0:4)
Course Title : LOW POWER VLSI DESIGN
Contact Period : Lecture :52 Hr, Exam: 3Hr  Weightage :CIE:50% SEE:50%

**Course Learning Objectives (CLO):**

At the end of the course the students should be able to:

1. Understand the basic knowledge of power dissipation in CMOS devices.
2. Estimate dynamic and leakage power components in a DSM VLSI circuit.
3. Differentiate the types of SRAMs/ DRAMs for low power applications.
4. Design low power arithmetic circuits and systems
5. Discuss the concepts of Low power Clock Distribution.

**Course Content**

**UNIT I**

*Introduction*: Sources of power dissipation, static power dissipation, active power dissipation designing for low power, circuit techniques for leakage power reduction. **Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.  **11Hrs**

**UNIT II**

Standard adder cells. CMOS adders architectures, low voltage low power design techniques, current mode adders.
Types of multiplier architectures, Braun, booth and Wallace tree multiplier and their performance comparsion.  **10Hrs**

**UNIT III**

Sources of power dissipation in SRAMs, low power SRAM circuit techniques, sources of power dissipation in DRAMs, low power DRAM circuit techniques

**Low Power Design Circuit level:** Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library.  **10Hrs**
UNIT IV
The increased delays of wires, new materials for wires and dielectrics, design methods taking into account interconnection delays, cross talk.

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. 10Hrs

UNIT V
Basic background on testing, unsuitable design techniques for safety critical applications, low power and safety operating circuits, case study – A low power subsystem design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. 11Hrs

TEXT BOOKS:

REFERENCE

Course Outcome (CO):
The student is able to
1. Identify clearly the sources of power consumption in a given VLSI circuit.
2. Analyze and estimate dynamic and leakage power components in a DSM VLSI circuit.
3. Choose different types of SRAMs/ DRAMs for low power applications.
4. Design low power arithmetic circuits and systems
5. Decide at which level of abstraction it is advantages to implement low power techniques in a VLSI system design.
Course Code: P18MECE23  Semester : II  (L:T:P:H: 4:0:0:4)

Course Title : REAL TIME SYSTEMS

Contact Period : Lecture :52 Hr,Exam: 3Hr  Weightage : CIE:50% SEE:50%

Course Learning Objectives (CLOs):
This Course aims to:
1. Describe a reference model of real time systems and its applications.
2. Characterize hard and soft real time systems.
3. Describes clock driven approach in safety critical applications.
4. Understand the concept of scheduler.
5. Understand basic multi-task scheduling algorithms for periodic, aperiodic, and sporadic tasks.
6. Analyze the real time issues in communication network.
7. Summarizes the control and data dependence among tasks.
8. Describes the task execution and synchronization on different processors.

Course Content

UNIT I

Hard Versus Soft Real Time Systems: Jobs and processors, release times, deadlines and timing constraints, hard and soft timing constraints, hard real time systems, soft real time systems.


Text: 2.1 to 2.5, 3.1 to 3.8  10 Hrs

UNIT II

Commonly Used Approaches To Real – Time Scheduling: Clock – Driven approach, weighted round – robin approach, priority – driven approach, dynamic versus static systems, effective release times and deadlines, optimality of the EDF nd LST algorithms, nanoptimality in validating timing constraints in priority driven systems, off – line versus on – line scheduling.

Clock – Driven Scheduling: notations and assumptions, static, timer driven scheduler, general structure of cyclic schedules, cyclic executives, improving the average response time of aperiodic jobs, scheduling sporadic jobs, practical considerations and generalizations, algorithm for constructing static schedules, pros and cons of clock driven scheduling.

Text: 4.1 to 4.9, 5.1 to 5.9  11 Hrs
UNIT III
Priority _ Driven Scheduling Of Periodic Tasks: static assumption, fixed priority versus dynamic priority algorithms, maximum schedulable utilization, optimality of the RM and DM algorithms, a schedulability test for fixed priority tasks with short response times, schedulability test for fixed priority tasks with arbitrary response times, sufficient schedulability conditions for the RM and DM algorithms, practical factors.
Text: 6.1 to 6.8

UNIT IV
Resources And Resource Access Control: assumptions on resources and their usage, effects of resource contention and resource access control, nonpreemptive critical sections, basic priority – inheritance protocol, basic priority – ceiling protocol, stack – based, priority – ceiling (ceiling – priority) protocol, use of priority – ceiling protocol in dynamic – priority systems, preemption – ceiling protocol, controlling accesses to multiple unit resources, controlling concurrent accesses to data objects.
Text: 8.1 to 8.10

UNIT V
Multiprocessor Scheduling Resource Access Control And Synchronization: model of multiprocessor and distributed systems, task assignment, multiprocessor priority – ceiling protocol, elements of scheduling algorithms for End – to End periodic tasks.
Text: 9.1 to 9.4, 11.1 to 11.4

TEXT BOOK

REFERENCE

Course outcomes(CO):
The student is able to
1. Outline hard and soft real time systems.
2. Summarizes the concept of clock driven scheduling and its practical considerations. Differentiate the fixed priority verses dynamic priority algorithms of periodic tasks. Interpret the effects of resource contention and resource access control.
3. Explain the model of multiprocessor and distributed systems.
4. Explain the priority based service disciplines for switched networks.
ELECTIVE III

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<td>Course Title : ARM Processors</td>
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<td>Contact Period : Lecture :52 Hr,Exam: 3Hr</td>
<td>Weightage :CIE:50% SEE:50%</td>
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Prerequisites:
The student should have undergone the course on basic embedded systems and microcontrollers architecture and programming

Course Learning Objectives (CLOs):
At the end of the course the students should be able to:

1. Understand general architecture of ARM processor
2. Thoroughly discuss architecture of Cortex family M3 & M4 Processors
3. Implement embedded systems using Cortex M3 & M4
4. Debug faults in the Cortex M# & M4 processor based systems
5. Highlight specialities of Cortex M3 & M4 processors
6. Choose processor based on the system specifications

Course Content

UNIT I
Technical Overview
General information about the Cortex_-M3 and Cortex-M4 processors, Features of the Cortex_-M3 and Cortex-M4 processors 10 Hrs

UNIT II
Introduction to the architecture: Architecture, Programmer’s model, Behavior of the application program status register (APSR), Memory system, Exceptions and interrupts
Memory systems: Overview of memory system features ,Memory map, Connecting the processor to memory and peripherals ,Memory requirements,Memory endianness , Data alignment and unaligned data access support , Bit-band operations, Default memory access permissions, Memory access attributes, Memory system in a microcontroller. 11 Hrs
UNIT III

Exceptions and Interrupts: Overview of exceptions and Interrupt types, Overview of interrupt management, Definitions of priority, Vector table and vector table relocation, Interrupt inputs and pending behaviors, Exception sequence overview, Details of NVIC registers for interrupt control, Details of SCB registers for exception and interrupt control, Details of special registers for exception or interrupt masking.

Interrupt latency and exception handling optimization, 11 Hrs

UNIT IV

Low Power and System Control Features
Low power designs, Low power features, Using WFI and WFE instructions in programming, Developing low power applications, The SysTick timer, Self-reset, CPU ID base register, Configuration control register, Auxiliary control register, Co-processor access control register

Memory Protection Unit (MPU)
Overview of the MPU, MPU registers, Setting up the MPU, Memory barrier and MPU configuration, Using sub-region disable, Considerations when using MPU, Other usages of the MPU, 10 Hrs

UNIT V

Fault Exceptions and Fault Handling
Overview of fault exceptions, Enabling fault handlers, Fault status registers and fault address registers, Analyzing faults, Faults related to exception handling, Lockup, Fault handlers

Introduction to the Debug and Trace Features
Debug and trace features overview, Debug architecture, Debug modes, Debug events, Breakpoint feature, Debug components introduction, Debug operations, 10 Hrs

TEXT BOOK


REFERENCE


Course Outcome (CO):

The student should be able to

1. Analyze embedded systems based on Cortex M3 & M4 processors
2. Describe Architecture of Cortex M3 & M4 processors
3. Discriminate ARM and other processors
4. Highlight important features of Cortex family processors
5. Explain Interrupt mechanism, fault handling, debug architecture, memory protection unit specific to Cortex M3 & M4 processors
Course Code: P18MECE242  |  Semester: II  |  (L:T:P:H: 3:0:2:5)
|-----------------|----------------|----------------|
Course Title: EMBEDDED SYSTEM DESIGN WITH FPGA

Contact Period: Lecture: 52 Hr, Exam: 3 Hr  |  Weightage: CIE: 50% SEE: 50%

Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to:
1. Provides basic knowledge of embedded system.
2. Explain the computer hardware and software.
3. Illustrate the concept of the SAYEH Design and Test.
4. Describe the concept of Field Programmable gate arrays.
5. Explain the embedded system design tools and design prototyping.
6. Describe the various concept of design of utility hardware cores.
7. Explain the concepts of embedded design steps.

Course Content

UNIT I

Computer Hardware And Software:


UNIT II

Field Programmable Devices:

Read Only Memory, Basic ROM Structure, NOR Implementation, Distributed Gates, Array Programmability, Memory View, ROM Variations, Programmable Logic Arrays, PAL Logic Structure, Product Term Expansion, Three-State Outputs, Registered Outputs, Commercial Parts, Complex Programmable Logic Devices, Altera's MAX 7000S CPLD, Field Programmable gate arrays, Altera's FLEX 10K DOGMA, Altera's cyclone DOGMA. 10 Hrs

UNIT III

Tools For Design And Prototyping:

UNIT IV

Design Of Utility Hardware Cores:

Design With Embedded Processors:

UNIT V


TEXT BOOK

1. Embedded Core Design with FPGAs, 1e, Zainalabedin Navabi, McGrawHill 2008

Course Outcomes (CO)

The student is able to

1. Explain the concept of Machine Language, Assembly Language, High-Level Language.
2. Analyze the concept of SAYEH Top-Level Testbench / Assembler.
3. Describe the structure of PLA and PAL arrays.
4. Explain the concept of Altera’s MAX 7000S CPLD.
5. Estimate the HDL Simulation and Synthesis.
ELECTIVE IV

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<tr>
<td>Course Title : System Verilog</td>
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<td>Contact Period : Lecture :52 Hr, Exam: 3Hr</td>
<td>Weightage : CIE:50% SEE:50%</td>
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**Course Learning Objectives (CLOs)**

After learning all the units of the course, the student is able to

1. Understand the basic knowledge of C, C++ and Verilog.
2. Describe the Verification basics, Testbenches, Layered Organization of Testbenches.
3. Explain the System Verilog data types and typedefs
4. Provide the basic understanding of System Verilog operators, loops, jumps, functions
5. Explain the system Verilog Class and Randomization.
6. Describe the various types of Interfaces.

**Course Content**

**UNIT I**

**Introduction to System Verilog:** System Verilog origins, Key System Verilog enhancements for hardware design.

**System Verilog Declaration Spaces:** Packages, $unit compilation-unit declarations, Declarations in unnamed statement blocks, Simulation time units and precision.

**System Verilog Literal Values and Built-in Data Types:** Enhanced literal value assignments, define enhancements, System Verilog variables, Using 2-state types in RTL models, Relaxation of type rules, Signed and unsigned modifiers, Static and automatic variables, Deterministic variable initialization, Type casting. **10 Hrs**

**UNIT II**

**System Verilog User-Defined and Enumerated Types:** User-defined types, Enumerated types, System Verilog Arrays, Structures and Unions: Structures, Unions, Arrays, The for each array looping construct, Array querying system functions, The $bits “size of” system function, Dynamic arrays, associative arrays, sparse arrays and strings.

**System Verilog Procedural Blocks, Tasks and Functions:** Verilog general purpose always procedural block, System Verilog specialized procedural blocks, Enhancements to tasks and functions. **11 Hrs**
UNIT III

**System Verilog Procedural Statements:** New operators, Operand enhancements, Enhanced for loops, Bottom testing do while loop, The for each array looping construct, New jump statements — break, continue, return. Enhanced block names ,Statement labels, Enhanced case statements, Enhanced if...else decisions.

**Modeling Finite State Machines with System Verilog:** Modeling state machines with enumerated types, Using 2-state types in FSM models. **10 Hrs**

UNIT IV

**SystemVerilog Design Hierarchy:** Module prototypes, Named ending statements, Nested (local) module declarations, Simplified netlists of module instances, Net aliasing, Passing values through module ports, Reference ports, Enhanced port declarations, Parameterized types.

**SystemVerilog Interfaces:** Interface concepts, Interface declarations, Using interfaces as module ports, Instantiating and connecting interfaces, Referencing signals within an interface, Interface modports, Using tasks and functions in interfaces, Using procedural blocks in interfaces, Reconfigurable interfaces, Verification with interfaces. **11 Hrs**

UNIT V

**A Complete Design Modeled with SystemVerilog:** SystemVerilog ATM example, Data abstraction, Interface encapsulation, Design top level: squat, Receivers and transmitters, Testbench.

**Behavioral and Transaction Level Modeling:** Behavioral modeling, Transaction level models via interfaces, Bus arbitration, Transactors, adapters, and bus functional models, More complex transactions. **10 Hrs**

TEXT BOOKS


REFERENCE

1. Sutherland, “System verilog for Design”, Springer publications
Course Outcome (CO):
The student should be able to

1. Apply the knowledge of the verilog language and digital system for design any application.
2. Analyze the various concepts of System Verilog data types, typedefs, operators, loops, jumps, functions.
3. Develop the system verilog code for sequential circuits. Structs, Unions, Packed and Unpacked Arrays, Semaphores and Mailboxes.
4. Design the system using system verilog constructs for the particular application.
5. Analyze the various types of Program blocks, Constrained Random variables, Coverage, Methods and interfaces, System Verilog assertion system functions.
Course Code: P18MECE252  Semester : II  (L:T:P:H: 3:0:2:5)

Course Title : DESIGN OF VLSI SYSTEMS

Contact Period : Lecture:52Hr,Exam:3Hr  Weightage:CIE:50% SEE:50%

Course Learning Objectives (CLOs)

After learning all the units of the course, the student is able to
1. Provide the basic knowledge of VLSI system design
2. Explain the concept of VLSI System Design Methodology and Chip Design Methods.
3. Provide the understanding of Design Capture Tools.
4. Highlight the concept of Data Path Sub System Design and Array Subsystem Design
5. Outline the concepts of Control Unit Design and Special Purpose Subsystems.
6. Provide the knowledge of Design Economics, VLSI System Testing & Verification

Course contents

UNIT I


Chip Design Methods: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System

UNIT II

UNIT III

**Data Path Sub System Design:** Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations.

**Array Subsystem Design:** SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays. 10Hrs

UNIT IV

**Control Unit Design:** Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.

**Special Purpose Subsystems:** Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc. 10Hrs

UNIT V

**Design Economics:** Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example

**VLSI System Testing & Verification:** Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan

**VLSI Applications:** Case Study: RISC microcontroller, ATM Switch, etc. 11Hrs

TEXT BOOKS


REFERENCE


**Course outcomes (CO):**

The student is able to

1. Explain the basics of VLSI System Design Methodology and Chip Design Methods.
2. Discuss the various concepts of Design Capture Tools.
3. Discuss the concept of Data Path Sub System Design and Array Subsystem Design.
4. Analyze the concepts of Control Unit Design and Special Purpose Subsystems.
5. Explain the basic concepts of Design Economics, VLSI System Testing & Verification.
Course Code: P18MECEL26  Semester : II  (L:T:P:H: 0:0:4:4)

<table>
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<tr>
<th>Course Title : VLSI DESIGN LABORATORY</th>
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<td>Contact Period:Lecture :42 hrs,Exam: 3hrs</td>
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**Course Learning Objectives (CLOs)**

After learning all the units of the course, the student is able to

1. Understand the basic knowledge of how to use CADENCE Tool for VLSI concepts.
2. Analyze the ASIC Design flow.
3. Design and Verify an inverter, Buffer, Transmission gate and Basic/universal gates using verilog code.
4. Design and Verify a Flip flops (RS, D, JK, MS, T) and Serial & Parallel adder using Verilog code.
5. Design and Verify the 4-bit counter [Synchronous & Asynchronous counter] using verilog code.

**Course Content**

A.VLSI Digital Design

(i) ASIC-Digital Design Flow

1. Write Verilog Code for the following circuits and their Test Bench for verification,
   - An inverter, Buffer and Transmission gate
   - Basic/universal gates
   - Flip flop -RS, D, JK, MS, T
   - Serial & Parallel adder
   - 5.4-bit counter [Synchronous & Asynchronous counter]
(ii) FPGA DIGITAL DESIGN

VLSI Front End Design programs:

1. Write Verilog code for the design of 8-bit
   - Carry Ripple Adder
   - Carry LookAhead adder
   - Carry Skip Adder
   - BCD Adder & Subtracter

2. Write Verilog Code for 8-bit
   - Array Multiplication (Signed and Unsigned)
   - Booth Multiplication (Radix-4)

3. Write Verilog code for 4/8-bit
   - Magnitude Comparator
   - LFSR
   - Parity Generator
   - Universal Shift Register

4. Write Verilog Code for 3-bit Arbitrary Counter to generate 0,1,2,3,6,5,7 and repeats.

5. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.

6. Design a FIFO and LIFO buffers in Verilog and Verify its Operation.

7. Design a coin operated public Telephone unit using Mealy FSM model with specified operations

Note: Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.
B. ANALOG DESIGN

Analog Design Flow:

1. Design an Inverter with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      - DC Analysis
      - Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for XX
   d. Extract RC and back annotate the same and verify the Design
   e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      - DC Analysis
      - AC Analysis
      - Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for XX
   d. Extract RC and back annotate the same and verify the Design.
   i) A Single Stage differential amplifier
* Appropriate specification should be given.

** Applicable Library should be added & information should be given to the Designer.

*** An appropriate constraint should be given

6. Design a simple 8-bit ADC converter using any one of the tools given above.

7. Design a simple NAND/NOR gate using any one of the tools given above. (Any other experiments may be added in supportive of the course)

**Course Outcome(CO):**

The student should be able to

1. Analyze the ASIC flow and FPGA Digital Design.

2. Apply the knowledge of the digital system to design of the schematic and layout in Cadence tools.

3. Develop 8-bit Carry Ripple Adder, Carry LookAhead adder and Carry Skip Adder using Verilog code.


5. Develop 8-bit Array Multiplication (Signed and Unsigned) and Booth Multiplication (Radix-4) using Verilog code.